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Abstract

In this thesis, novel technologies of GaAs HBTs for high-speed and low-power applications have been studied. A series of the novel technologies dealt with analyses of material properties, fabrication processes, device designs, and circuit applications, those were developed to overcome the crucial problems of GaAs HBTs for high-speed and low-power operations. The technologies demonstrate great potential of GaAs HBTs for high-speed and low-power integrated-circuit applications.

In chapter 2, fundamental device physics and figures-of-merits of HBTs are reviewed to understand the relations between material properties, device designs, and device characteristics. The characteristics of conventional InGaP/GaAs HBTs were analyzed in detail and discussed to specify the guides to their high-speed and low-power operations.

In chapter 3, the characteristics of InGaP/GaAs HBTs with a heavily-doped and thin base are studied in detail in order to optimize the base layer design for high-speed operations. The analysis of the current gain h_{FE} on the base doping concentration N_B revealed that the h_{FE} at an N_B above $3 \times 10^{20} \text{ cm}^{-3}$ drastically decreased as N_B increased because of the reduction of the effective hole barrier height, which was explained analytically and experimentally by considering the bandgap narrowing and the Fermi level in accordance with the Fermi-Dirac distribution. The analysis of the base transit time τ_B showed that the τ_B exhibited a quadratic dependence on the base thickness W_B at a W_B larger than 30 nm, whereas the τ_B tended to show a linear dependence at a smaller W_B .

In chapter 4, a novel device structure and the corresponding process technology are proposed to reduce the parasitic capacitance under the base contact pad region. The devices were fabricated by using WSi/Ti as the base electrode and by burying SiO₂ in the extrinsic collector. The specific contact resistance ρ_c of WSi for p -GaAs was $2 \times 10^{-6} \Omega \cdot \text{cm}^2$ at an N_B of $1 \times 10^{20} \text{ cm}^{-3}$, which was dramatically reduced to $3 \times 10^{-7} \Omega \cdot \text{cm}^2$ by inserting a 5-nm Ti film between the interface. The low ρ_c made it possible to reduce the optimum base contact width for achieving both high f_T and high f_{\max} to less than 0.4 μm without the large increase in the base resistance. The simultaneous reduction of both the emitter size and the extrinsic collector capacitance effectively improved the high-frequency performance of small-scale

GaAs HBTs, which operated at higher speed and lower current than the conventional HBTs: an HBT with an emitter size S_E of $0.6 \mu\text{m} \times 4.6 \mu\text{m}$ provided an f_T of 138 GHz and an f_{max} of 275 GHz at a collector current I_C of 4 mA.

In chapter 5, the advanced high-frequency performance of small-scale InGaP/GaAs HBTs was demonstrated by refining the process technology and the device design. A double photoresist coating with a high-temperature reflow improved the uniformity of the buried SiO_2 , and improved the thickness of the buried SiO_2 by 25%. The thick buried SiO_2 together with the reduction of the base electrode area enabled the 50% reduction of the parasitic capacitance at the buried SiO_2 region. The refinements improved the high-frequency performance of small-scale HBTs: an HBT with an S_E of $0.5 \mu\text{m} \times 4.5 \mu\text{m}$ exhibited a f_T of 156 GHz and a f_{max} of 255 GHz at an I_C of 3.5 mA; an HBT with an S_E of $0.25 \mu\text{m} \times 1.5 \mu\text{m}$ exhibited a f_T of 114 GHz and a f_{max} of 230 GHz for at an I_C of 0.9 mA. A 1/8 static frequency divider fabricated by using the developed HBTs operated at a maximum operation frequency of 39.5 GHz with power consumption per flip-flop of 190 mW, which is about 2/3 of those of previously-reported GaAs-HBT static frequency dividers. A transimpedance amplifier had a transimpedance gain of $46.5 \text{ dB} \cdot \Omega$ with a 41.6-GHz bandwidth. The power consumption was 150 mW, which is less than half that of the same type of amplifier previously reported.

In chapter 6, GaAs HBTs with a pseudomorphic, fully-strained GaAsSb base were demonstrated for reducing the turn-on voltage V_{on} in GaAs HBTs. The V_{on} of the GaAs/GaAs_{0.9}Sb_{0.1} HBTs was reduced by about 0.1 V compared to that of the InGaP/GaAs HBT. The reduction was in good agreement with the bandgap reduction of the base layer. Owing to the fully-strained GaAsSb without misfit dislocations, the maximum current gain of 35 was attained. The collector current blocking effect was insignificant due to the small conduction band discontinuity ΔE_C . The potential barrier height of metal/ p -GaAsSb tended to decrease as increasing the Sb composition. As a result, a specific contact resistance as low as $6 \times 10^{-7} \Omega \cdot \text{cm}^2$ was achieved at p -GaAs_{0.9}Sb_{0.1} with a relatively low base doping level of $2 \times 10^{19} \text{ cm}^{-3}$. In contrast, the hole mobility of GaAsSb was increased as the Sb composition increased.

In chapter 7, the accomplishments and conclusions of this thesis are summarized, and the remaining problems and suggestions for the future work are given.

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Chapter 1

Introduction

1.1 Background

It is no exaggeration to say that the recent progress in communication systems has been achieved largely due to advances in semiconductor technology. The foundation of the dominant high-speed integrated circuit (IC) technology has been provided by Si bipolar devices and GaAs metal semiconductor field effect transistors (MESFETs), and, along with their development, the communication market has been grown continuously and phenomenally. And now, the information technology is quickly becoming an integral part of our lives not only in the workplace but also at home and, consequently, the carrying capacity of communication systems is tremendously increasing in order to handle a large amount of information. Under the circumstances, the development of up-coming communication systems, such as advanced microwave/millimeter-wave wireless communication systems and large capacity optical-fiber telecommunication systems, is accelerated and, hence, the practical use of ultra-high-speed devices, such as high electron mobility transistors (HEMTs) and heterojunction bipolar transistors (HBTs), is promptly demanded.

1.2 Heterojunction Bipolar Transistors

1.2.1 Fundamental theory and characteristics

Heterojunction bipolar transistors (HBTs) based on III-V semiconductor materials are one of the promising devices for up-coming high-speed applications. III-V HBTs have unique and inherent advantages in performance over Si bipolar devices and III-V MESFETs or HEMTs [1]. Figure 1-1 shows the energy band diagram and the flow of electrons and holes of n - p - n HBTs. The difference from homojunction bipolar transistors (BJTs) is that the bandgap of the emitter is larger than that of the base. The large valence band discontinuity at the emitter-base junction functions as the barrier for the base-to-emitter hole injection, whereas the conduction band discontinuity does not block emitter-to-base electron flow significantly. The hole barrier allows the base doping concentration to be much higher than the emitter doping concentration without sacrificing the emitter injection efficiency. As a consequence, base doping concentrations can be set higher in HBTs than in BJTs. The low emitter doping reduces the emitter-base capacitance, and, in addition, the high base doping decreases the base resistance; both of which are useful for improving the high-frequency performance of bipolar transistors [2].

Compared to MESFETs and HEMTs, HBTs have much higher power handling capability, higher current driving capability and lower $1/f$ noise characteristics, with high-frequency and high-speed performance. The high power handling capability resulting from high power density operations enables small die size for a given power requirement. This is important for power transistors especially for millimeter wave ranges, since keeping phase uniformity in active devices is a key issue for high-frequency devices. The high current drive capability is a necessary condition for high-speed digital circuits to charge and discharge load capacitance such as wiring capacitance. The low $1/f$ noise characteristic of HBTs is attractive for oscillator applications since low-frequency noise such as $1/f$ noise generates phase noise of oscillators due to nonlinear characteristics of transistors. Furthermore, HBTs have better threshold voltage control with better uniformity because the turn-on voltage primarily corresponds to the bandgaps of the emitter and base materials. In addition, intrinsic transit

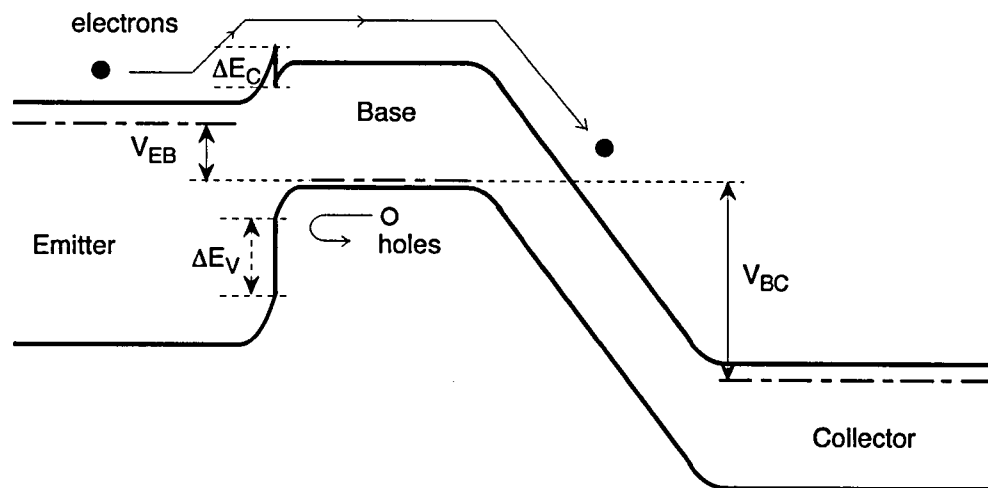


Fig. 1-1. Energy band diagram and the flow of electrons and holes of n - p - n HBT.

time determined by the base and collector layer thicknesses can be readily controlled in the nanometer range by using epitaxial growth technologies. These can relax the process margin in the HBT fabrication than that in FETs, particularly in terms of lithographic requirements, resulting in higher yields and therefore lower costs.

In comparison with Si bipolar devices such as Si BJTs and SiGe HBTs, on the other hand, III-V HBTs offer further advantages over Si-based material systems: i.e., higher electron mobility with a potential for transient velocity overshoot effects in III-V materials enable to improve cutoff frequency at a similar vertical device scale. In addition, III-V HBTs have a higher breakdown voltage than Si bipolar devices, increasing cutoff frequency by reducing the vertical scale of the collector layer with keeping high collector-emitter breakdown voltages (BV_{CEO}). Furthermore, compact, monolithically integrated microwave circuits can be fabricated as a complete unit by using semi-insulating substrates, which help to reduce pad parasitics and, thus, allow convenient integration of devices.

All these features make III-V HBTs the "device of choice" for many circuit designers developing cutting-edge integrated circuits for ultra-high-speed applications.

1.2.2 Overview of development history

The fundamental theory of an HBT was proposed by Shockley in 1948 as stated in Claim 2, US Patent 2 569 347 [3], and the operation principles, advantages and possible applications were first discussed by Kroemer in detail in 1957[4]. However, HBTs were neglected for a certain period because of the rapid development of simple homojunction bipolar devices and the limitations of hetero-epitaxy techniques.

The first truly operational HBT was realized in 1969; the emitter-base heterojunction was GaAs/Ge grown by Liquid Phase Epitaxy (LPE) [5]. It resulted in the fabrication of a bipolar device with a current gain larger than 10 with the base doping ($5 \times 10^{19} \text{ cm}^{-3}$) by three orders of magnitude higher than the emitter doping ($5 \times 10^{16} \text{ cm}^{-3}$).

The successful development of the HBT technology was achieved in the 1970's by the tremendous progress made in high-precision epitaxial growth systems for III-V semiconductor materials. Two advanced growth techniques, molecular beam epitaxy (MBE) [6] and

metal-organic chemical vapor deposition (MOCVD) [7], provided the atomic level control in layer thickness, chemical composition, and doping level needed for useful heterojunctions. The AlGaAs/GaAs system was the first beneficiary of the heterostructure materials, and the first AlGaAs/GaAs HBTs were fabricated in 1972 [8].

With the remarkable progress of high-quality epitaxial growth technology, HBTs began to be researched and developed as actual devices for practical use by the mid-1980's [9]. By the end of 1980's, the advanced process technologies improved the discrete device characteristics and circuit performance of AlGaAs/GaAs HBTs, which demonstrated GaAs HBTs as an attractive device for future ultra-high-speed applications [10].

At that time, InP HBTs, such as InAlAs/InGaAs HBTs and InP/InGaAs HBTs grown on InP substrates, have also emerged as potential candidates for high-speed applications because of their the excellent carrier transport properties [11]. The first Si/SiGe HBTs were also reported at that time [12].

In the 1990's, devices and circuits of InP HBTs and SiGe HBTs have shown some very promising results with excellent high-speed performance [13]. Besides, the epitaxial technology of InGaP on GaAs, which has excellent material properties, greater reliability, and ease of fabrication using selective etching compared to AlGaAs, was matured, and, as a result, InGaP/GaAs HBTs have attracted much interest as a potential replacement for AlGaAs/GaAs HBTs [14-17].

1.2.3 Comparison of material and characteristics

The limiting factor for bipolar technologies is in the collector profile and material structure; namely, the collector-emitter breakdown voltage BV_{CEO} can be traded off for cutoff frequency f_T related to the collector thickness. Therefore, InP HBTs are more attractive than SiGe and GaAs HBTs for the high-speed applications because of the superior carrier transport properties of InGaAs used as the collector layer [18]. Figure 1-2 illustrates how f_T changes with BV_{CEO} [19]. For a given breakdown voltage, InP HBTs are faster than SiGe and GaAs HBTs. This is due to the high electron mobility of InGaAs, which overcomes the demerit of a low breakdown field. This indicates the potential of InP HBTs for ultra-high-speed

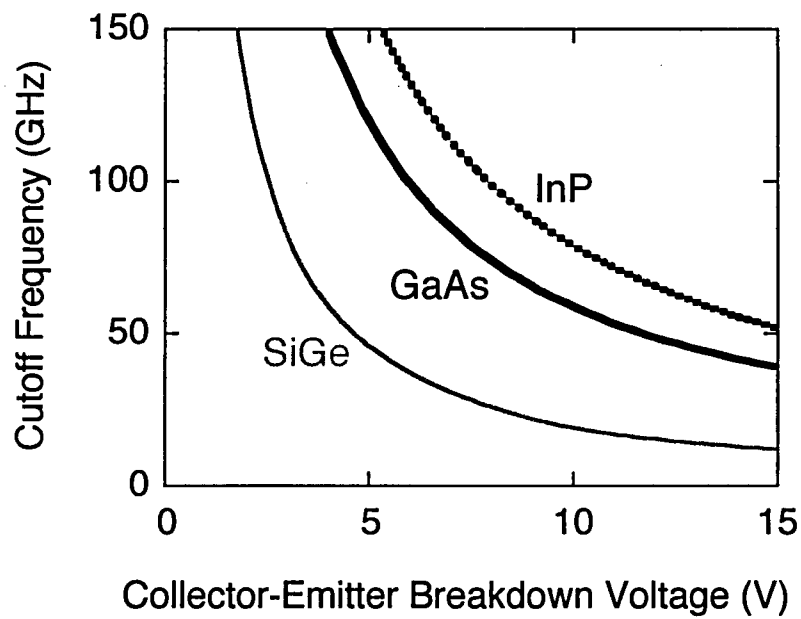


Fig. 1-2. Comparison of cutoff frequency as a function of breakdown voltage between SiGe, GaAs, and InP HBTs.

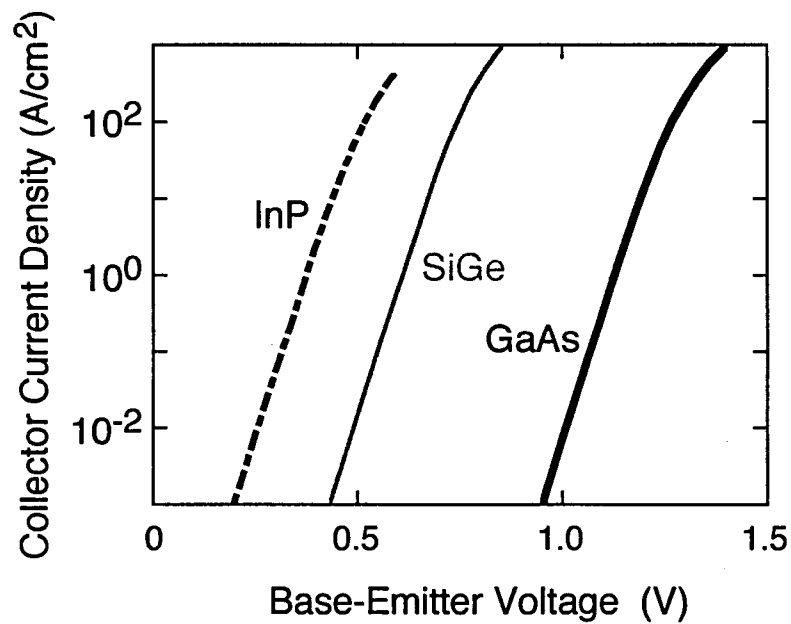


Fig. 1-3. Comparison of current-voltage characteristics between SiGe, GaAs, and InP HBTs.

applications.

InP HBTs have another advantage of a low turn-on voltage. Comparison of current-voltage characteristics between III-V HBTs and SiGe HBTs is shown in Fig. 1-3 [19]. Since the bandgap of InGaAs used as the base layer of InP HBTs is generally narrower than SiGe and GaAs [18,20], InP HBTs can operate at lower voltages with higher current densities. This indicates that InP HBTs are also ideal for low-voltage and thus low-power applications.

In contrast, Si bipolar devices remain highly competitive because of the aggressive submicron scaling. Figure 1-4 shows the comparison of typical device dimension between SiGe HBTs and III-V HBTs. Typical emitter width and length of self-aligned SiGe HBTs are 0.1-0.2 μm and 1-2 μm , respectively [21,22]. To the contrary, typical emitter width and length of III-V HBTs are 1-2 μm and 5-10 μm , respectively, the large values of which are due to the mesa-structure devices. As a result, the large device dimension of III-V HBTs requires larger collector currents than SiGe HBTs in order to operate at high frequency. Typical dependence of cutoff frequency on collector currents between SiGe HBTs and III-V HBTs are compared in Fig. 1-5 [22-24]. Although the peak cutoff frequency of SiGe HBTs is lower than that of III-V HBTs, SiGe HBTs can operate at higher cutoff frequencies with lower collector currents, indicating that SiGe HBTs are suitable for low-power applications.

1.3 Subject of This Research

As stated in the previous section, the device dimensions of III-V HBTs are relatively large and, thus, large collector currents are necessary in order to operate at high frequency. This causes the large power dissipation as well as thermal-management problems when they are applied to highly integrated chips such as those used in high-speed communications. Hence, submicron scaling for III-V HBTs is a crucial issue to achieve both high-speed and low-power operations simultaneously.

For the fabrication of small-scale III-V devices, GaAs is more attractive material than InP because the process technology of InP has not been matured sufficiently and, thus, difficult to obtain submicron scaling with high processing yields. In addition, InP wafers have

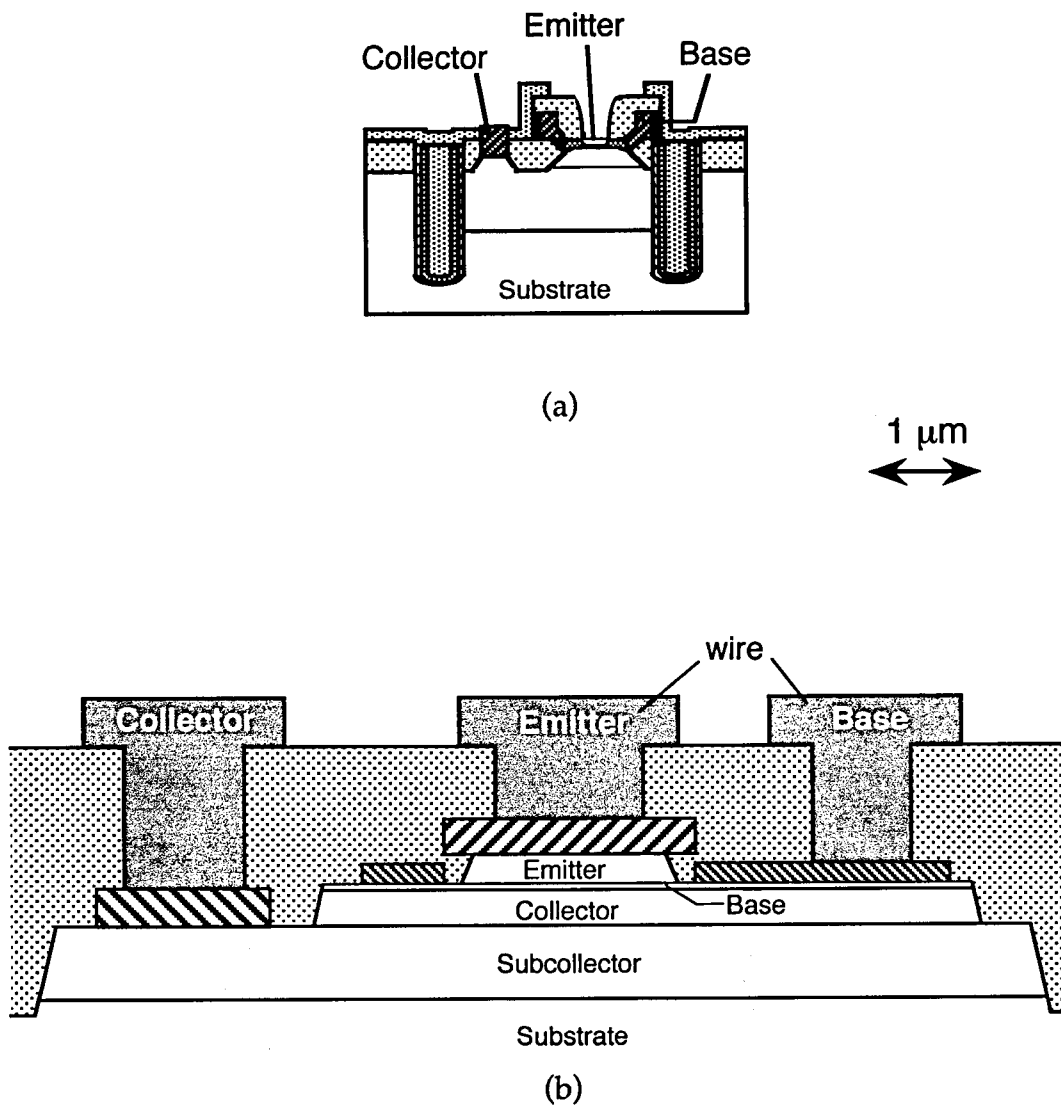


Fig. 1-4. Comparison of typical device dimension between (a) SiGe HBT and (b) III-V HBT.

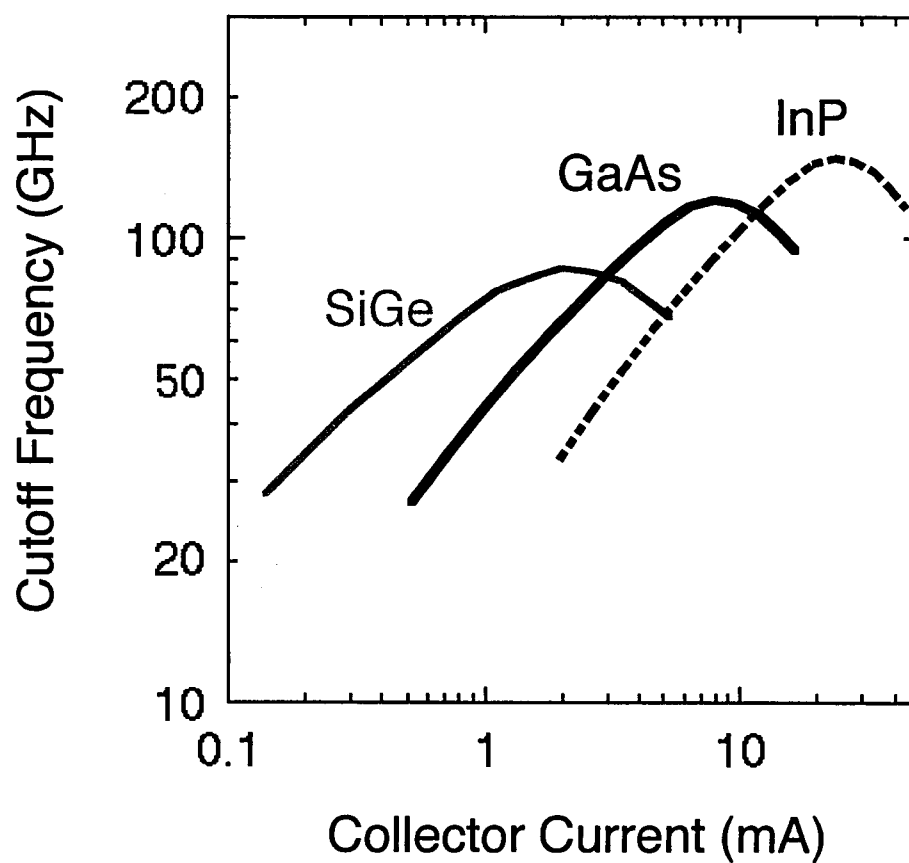


Fig. 1-5. Dependence of high-frequency characteristics on collector currents for SiGe, GaAs, and InP HBT.

the disadvantages of brittleness, unavailability of large-diameter wafers, high substrate cost, leading to higher production costs. In contrast, the process technology of GaAs has been matured enough to obtain high processing yields with low production costs, which is suitable to promptly reply the urgent demand for the practical use of high-speed applications.

Accordingly, this study focused on GaAs HBTs emerged as valuable devices and attractive candidates for high-speed and low-power applications. Although carrier transport properties of GaAs is inferior to InGaAs, the smaller Auger recombination coefficient of GaAs than InGaAs enables to attain a higher base doping level without sacrificing the current gain [25,26]. Hence, the lower base resistance than that obtainable in InP HBTs can be achieved even reducing the base thickness. This implies that GaAs HBTs have a possibility to attain higher frequency performance than InP HBTs by an appropriate design of the base layer.

To date, GaAs HBTs with high cutoff frequency f_T over 100 GHz [27] and high maximum oscillation frequency f_{max} over 200 GHz [28,29] have been reported. However, these HBTs have considerably large device dimensions and, thus, require larger collector currents in order to operate at high frequency, as stated previously. Although small-scaled GaAs HBTs with emitter areas of equal to or smaller than $1 \mu\text{m}^2$ have been demonstrated, their high-frequency characteristics were considerably deteriorated as the emitter size was scaled down [30-32]. To achieve high-speed, low-power IC operation with GaAs HBTs, therefore, it is critical to develop process technology and device design for scaling down of the device dimension without sacrificing the high-frequency performance.

When the emitter size of GaAs HBTs with AlGaAs emitter is scaled down, peripheral recombination currents around the emitter becomes a significant problem. In AlGaAs/GaAs HBTs, the exposed emitter periphery and the extrinsic base surface are passivated by stable oxides, which have very high recombination velocities and thus increase the peripheral recombination current. This gives rise to the current gain reduction as the emitter size is scaled down, known as the emitter size effect [33]. Although the peripheral currents can be reduced by introducing depleted AlGaAs surface passivation layers, so-called ledge passivation [34,35], the surface recombination velocity of AlGaAs is influenced by the process or the oxidation of AlGaAs, limiting the suppression of the emitter size effect [36,37]. Furthermore, AlGaAs/GaAs HBTs have another problem for low-power applications; i.e.,

higher Al composition to increase the valence band discontinuity ΔE_V for utilizing higher base doping also increases the conduction band discontinuity ΔE_C and, consequently, increases the turn-on voltage [38]. The increase of the turn-on voltage can be suppressed by introducing a compositionally graded AlGaAs layer. However, the graded layer adversely increases not only the hole injection into the emitter but also the space charge recombination [39,40], degrading both current gain and the effect of the ledge passivation [41].

Accordingly, InGaP was mainly utilized as the emitter material of GaAs HBTs in this study. InGaP/GaAs HBTs have gradually attracted much interest as a potential replacement for AlGaAs/GaAs HBTs because of ease of fabrication using selective etching and greater reliability [14,42,43]. Besides, InGaP has excellent material properties; i.e., smaller surface recombination velocity than that of AlGaAs [36], and smaller ΔE_C and larger ΔE_V of InGaP/GaAs than those of AlGaAs/GaAs heterojunction [44,45]. These properties suggest a potential of small-scale InGaP/GaAs HBTs with a low turn-on voltage. However, the study of InGaP/GaAs HBTs for use in high-speed and low-power applications has not been examined sufficiently. To fully exploit InGaP/GaAs HBTs as high-speed and low-power devices, therefore, it is indispensable to reveal the correlations between material properties, device designs, and device characteristics.

A large turn-on voltage of GaAs HBTs compared to SiGe and InP HBTs, as shown in Fig. 1-3, is also a key issue to be solved. The large turn-on voltage is caused by the large bandgap E_G of GaAs (1.42 eV) used as the base layer. This limits the minimum operating voltage and, thus, causes the increase in the power consumption of ICs using GaAs HBTs. Hence, narrower E_G material for the base layer should be developed for low-power operations.

1.4 Outline of Thesis

According to the issues mentioned in the previous section, GaAs HBT technologies for high-speed and low-power applications are studied in this thesis. The outline of the thesis is described as follows.

Chapter 2 reviews fundamental device physics and figures-of-merits of HBTs to

understand the relations between material properties, device designs, and device characteristics. The characteristics of InGaP/GaAs HBTs and the guides to their high-speed and low-power operations are also discussed.

Chapter 3 deals with the characterization of InGaP/GaAs HBTs with a heavily-doped and thin base. The dominant factor of determining the current gain at the extremely high doping level above $1 \times 10^{20} \text{ cm}^{-3}$ is elucidated. The influences of the base thickness on DC and high-frequency characteristics are also described.

In chapter 4, a novel device structure and the corresponding process technology are presented. An HBT with WSi/Ti base electrode and buried SiO₂ in the extrinsic collector is proposed to reduce the parasitic capacitance under the base contact pad region. The excellent high-frequency characteristics at low collector current operations of the proposed GaAs HBTs are also presented.

In chapter 5, refinements of the process technology and the device design for the further reduction of the parasitic capacitance are described. The further improvement of high-frequency characteristics in small-scaled InGaP/GaAs HBTs is demonstrated. The capability of the developed HBTs for high-speed and low-power integrated circuits is also investigated by applying them to 1/8 static frequency dividers as digital circuits and transimpedance amplifiers as analog circuits.

Chapter 6 describes the characteristics of GaAs HBTs with a pseudomorphic, fully-strained GaAsSb base. The reduction in turn-on voltage of the GaAs/GaAsSb/GaAs double heterojunction bipolar transistors (DHBTs) is demonstrated. The current gain, the offset voltage, and characteristics related to the base resistance are also described.

Chapter 7 summarizes the accomplishments and conclusions of this thesis, and describes remaining problems and suggestions for the future work.

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Chapter 2

Fundamentals of InGaP/GaAs HBTs and Guides to Their High-Performance Operations

2.1 Introduction

HBTs with InGaP/GaAs material systems were proposed by Kroemer in 1982 [1], and the first InGaP/GaAs HBTs were demonstrated in 1985 [2]. In the 1990s, InGaP/GaAs HBTs have gradually attracted much interest as a potential replacement for AlGaAs/GaAs HBTs. This is because InGaP/GaAs HBTs have excellent material properties, greater reliability, and ease of fabrication using selective etching in comparison with AlGaAs/GaAs HBTs [3-8].

To fully exploit InGaP/GaAs HBTs for high-speed and low-power applications, it is necessary to understand the influence of the device designs on their characteristics in detail. In this chapter, fundamental characteristics of InGaP/GaAs HBTs are evaluated in order to obtain the guide for their high performance operations. Firstly, fundamental device physics and figures-of-merits of HBTs are reviewed in order to understand the correlations between material properties, device designs, and device characteristics. Then, InGaP/GaAs HBTs with conventional device structure are fabricated and evaluated in order to understand the fundamental device characteristics. The results are analyzed to reveal the significant issues to be solved for high-speed and low-power operations of InGaP/GaAs HBTs. Based on these

results, the guides to their high-performance operations are discussed and specified.

2.2 Device Physics and Figures-of-Merits of HBTs

2.2.1 Analysis of DC operation

The schematic cross-section of an $n\text{-p}\text{-n}$ HBT with the flow of electrons and holes is shown in Fig. 2-1. The operational principles of HBTs are almost same as the conventional bipolar transistors except that a wide bandgap material is used as the emitter. The DC currents flowing in the HBT shown in Fig. 2-1 are given below:

I_{Ee} : injection current of electrons from the emitter into the base;

I_{Bh} : injection current of holes from the base into the emitter;

I_{Bbr} : bulk recombination current in the quasi-neutral base region;

I_{Bd} : recombination current in the emitter-base depletion region;

I_{Bp} : peripheral recombination current around the emitter-base junction.

When the emitter-base junction is a graded heterojunction, I_{Ee} is given by [9]

$$I_{Ee} \cong qS_E \frac{D_n}{L_n} \frac{n_{iB}^2}{N_B} \frac{1}{\tanh(W_B/L_n)} \exp\left(\frac{qV_{BE}}{kT}\right), \quad (2-1)$$

where S_E is the emitter size, D_n and L_n the diffusion coefficient and diffusion length of electrons in the base, respectively, n_{iB} the intrinsic carrier concentration of the base, N_B the base concentration, W_B the base thickness, and V_{BE} the bias voltage at the emitter-base junction. Assuming that electron transport in the base obeys the conventional diffusion model, the base transport factor β is given by

$$\beta = \frac{1}{\cosh(W_B/L_n)} \cong 1 - \frac{W_B^2}{2L_n^2}, \quad (2-2)$$

and, as a result, the collector current I_C is expressed as

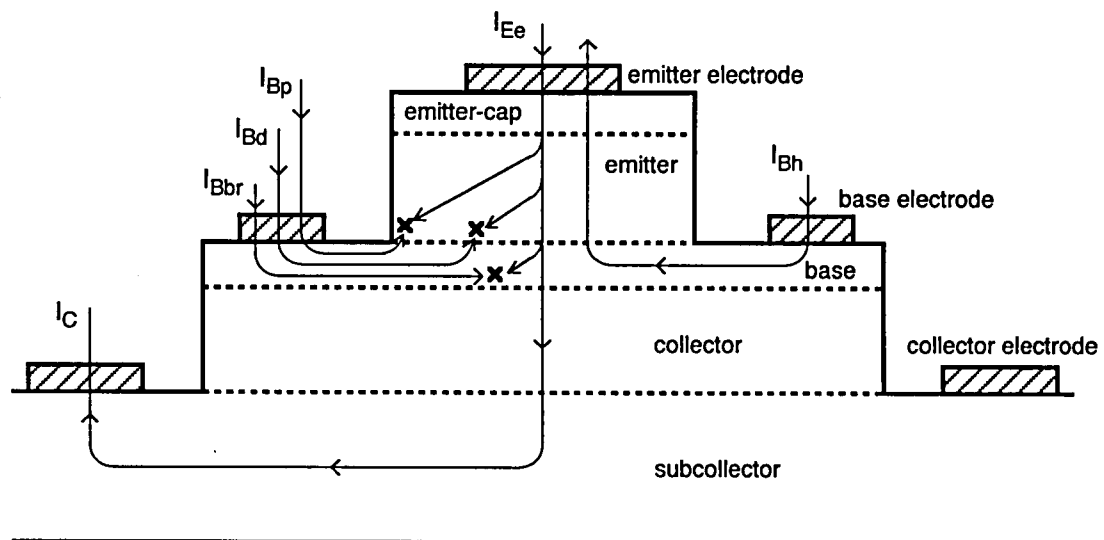


Fig. 2-1. Schematic cross-section of $n-p-n$ HBT with the flow of electrons and holes.

$$\begin{aligned}
I_C = \beta I_{Ee} &\cong q S_E \frac{D_n}{L_n} \frac{n_{iB}^2}{N_B} \frac{1}{\sinh(W_B/L_n)} \exp\left(\frac{qV_{BE}}{kT}\right) \\
&\cong q S_E \frac{D_n}{W_B} \frac{N_{CB} N_{VB}}{N_B} \exp\left(-\frac{E_{gB}}{kT}\right) \exp\left(\frac{qV_{BE}}{kT}\right),
\end{aligned} \tag{2-3}$$

where N_{CB} and N_{VB} are the effective densities of states in the conduction and valence bands in the base, respectively, and E_{gB} is the bandgap of the base. Equation (2-3) indicates that the saturation current and, thus, the turn-on voltage V_{on} of HBTs are determined by the material properties of the base layer, mainly E_{gB} .

When the emitter-base junction is an abrupt heterojunction with small conduction band discontinuity ΔE_C , I_C can be written as [1]

$$I_C \cong q S_E \frac{D_n}{W_B} \frac{N_{CB} N_{VB}}{N_B} \exp\left(-\frac{E_{gB} + \Delta E_C}{kT}\right) \exp\left(\frac{qV_{BE}}{kT}\right). \tag{2-4}$$

Equation (2-4) indicates that V_{on} for an abrupt heterojunction is about ΔE_C higher than that for a graded heterojunction. If the ΔE_C is much larger than kT , I_C is approximately given by the Richardson expression based on the thermionic emission theory written as [9,10]

$$I_C \cong A S_E T^2 \exp\left(-\frac{E_{gB} + \Delta E_C}{kT}\right) \exp\left(\frac{qV_{BE}}{kT}\right), \tag{2-5}$$

where A is the Richardson constant for thermionic emission. Equations (2-4) and (2-5) suggest that large ΔE_C as well as a wide bandgap base material increases the V_{on} of HBTs.

The common-emitter current gain h_{FE} of HBTs is expressed as [1]

$$h_{FE} = \frac{I_C}{I_B} = \frac{\beta I_{Ee}}{I_{Bh} + I_{Bbr} + I_{Bd} + I_{Bp}}. \tag{2-6}$$

When all recombination currents are negligible, i.e., $\beta \sim 1$, the h_{FE} of HBTs with a graded heterojunction is determined by the emitter injection efficiency, given by [1,9]

$$h_{FE} \cong h_{FEh} = \frac{I_{Ee}}{I_{Bh}} = \frac{L_p D_n N_E n_{iB}^2}{L_n \tanh(W_B/L_n) \cdot D_p N_B n_{iE}^2} \cong \frac{L_p D_n N_E N_{CB} N_{VB}}{W_B D_p N_B N_{CE} N_{VE}} \exp\left(\frac{\Delta E_G}{kT}\right), \tag{2-7}$$

where L_p and D_p are the diffusion length and diffusion coefficient of holes in the emitter, N_E the emitter doping concentration, n_{iE} the intrinsic carrier concentration of the emitter, N_{CE} and N_{VE} the effective densities of states in the conduction and valence bands in the emitter, respectively, and ΔE_G the bandgap difference between the emitter and the base. If the heterojunction is abrupt with a relatively small ΔE_C , ΔE_G in Eq. (2-7) is replaced by the valence band discontinuity ΔE_V [11]. In homojunction bipolar transistors, ΔE_G is almost 0 and thus N_E must be higher than N_B to obtain an adequate current gain. In contrast, HBTs can set a relatively large ΔE_G . For example, ΔE_G of an $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}/\text{GaAs}$ heterojunction is 0.37 eV, and ΔE_G of an InGaP/GaAs heterojunction is 0.42 – 0.48 eV. As a result, HBTs can have a very high current gain even though N_B is higher than N_E . Therefore, the I_{bh} in HBTs can be negligible; in other words, the current gain is determined by the recombination currents.

When the bulk recombination current is dominant, the current gain is expressed as [9]

$$h_{FE} \cong h_{FEbr} = \frac{I_C}{I_{Bbr}} = \frac{I_C}{I_{Ee} - I_C} = \frac{I_C}{I_C/\beta - I_C} = \frac{1}{\cosh(W_B/L_n) - 1} \cong \frac{2L_n^2}{W_B^2}. \quad (2-8)$$

This equation suggests that the current gain is mainly determined by the design of the base layer such as the base doping concentration and the base thickness. On the other hand, when the dominant recombination currents are caused by recombination centers such as defects or surface traps, the current gain is given by [12]

$$h_{FE} \cong h_{FEdp} = \frac{I_C}{I_{Bd} + I_{Bp}} = \left\{ \frac{J_{Bds}}{J_{Cs}} \exp \left[\left(\frac{1}{n_1} - 1 \right) \left(\frac{qV_{BE}}{kT} \right) \right] + \frac{J_{Bps}}{J_{Cs}} \exp \left[\left(\frac{1}{n_2} - 1 \right) \left(\frac{qV_{BE}}{kT} \right) \right] \cdot \frac{L_E}{S_E} \right\}^{-1}, \quad (2-9)$$

where

$$I_C = S_E J_{Cs} \exp \left(\frac{qV_{BE}}{kT} \right), \quad (2-10)$$

$$I_{Bd} = S_E J_{Bds} \exp \left(\frac{qV_{BE}}{n_1 kT} \right), \quad (2-11)$$

and

$$I_{Bp} = L_E J_{Bps} \exp\left(\frac{qV_{BE}}{n_2 kT}\right). \quad (2-12)$$

Here J_{Cs} , J_{Bds} , and J_{Bps} are the saturation current densities of the collector current, the recombination current in the depletion regions, and the peripheral recombination current, respectively, L_E is the length of the emitter periphery, and n_1 and n_2 are the ideality factors [9]. The value of n_1 is almost equal to 2, whereas n_2 varies between 1 and 2 depending on the conditions of the surface recombination at both the emitter periphery and extrinsic base regions [13]. If the peripheral recombination currents are dominant in particular, the current gain decreases as the emitter size is scaled down. This phenomenon is called as the emitter size effect, and becomes a serious problem of small-emitter-area HBTs [14].

2.2.2 High-frequency figures-of-merits

High-frequency characteristics of transistors are commonly evaluated by the current gain cutoff frequency f_T and the maximum oscillation frequency f_{max} , both of which have gained wide acceptance as appropriate benchmarks for characterizing the high-speed potential of a device [15,16]. The f_T is defined as the frequency at which the small-signal short-circuit current gain h_{21} is unity, relating the highest clock rate at which the device can operate. The f_{max} is the maximum frequency that the device can provide power gain. These two microwave figures-of-merits are extrapolated by device parameters which are characterized by fitting the measured s -parameters to a small-signal equivalent circuit model. Figure 2-2 shows a standard T-model of a small-signal equivalent circuit, which is appropriate to HBTs [17,18]. In this model, the base transport factor at high frequencies $\alpha(\omega)$ is expressed as

$$\alpha(\omega) = \frac{\alpha_0}{1 + j\omega/\omega_\alpha} \exp(-j\omega\tau), \quad (2-13)$$

where α_0 is the dc value of the base transport factor, $\omega_\alpha (= 2\pi f_\alpha)$ the -3-dB frequency for the base transport factor, and τ the delay time associated with the base transit time τ_b and the collector transit time τ_c . Based on this model, the relations between device parameters and

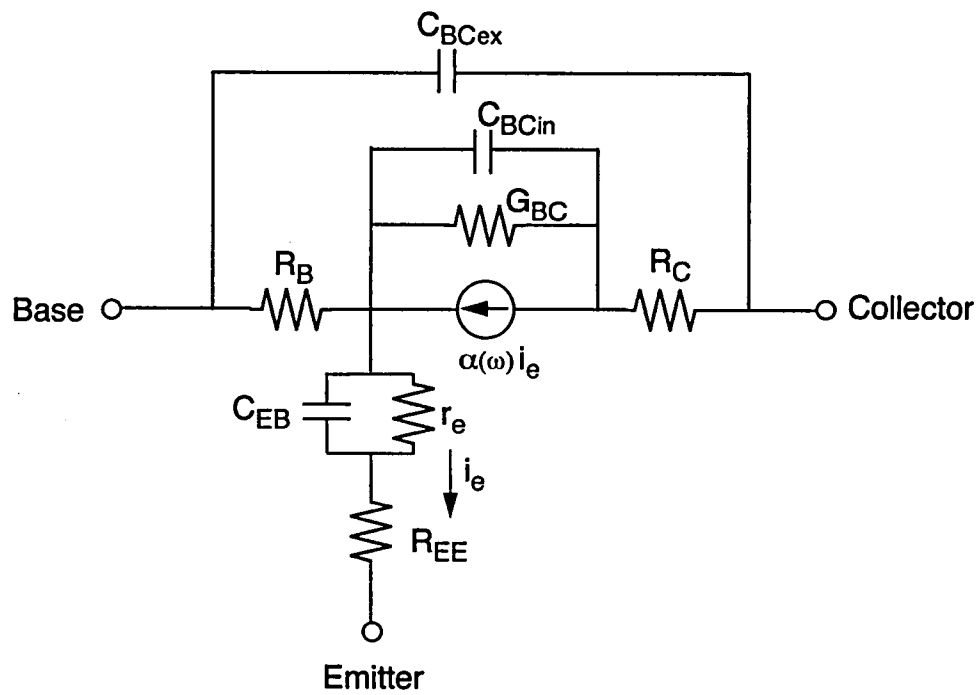


Fig. 2-2. Standard T-model of small-signal equivalent circuit for HBT.

the microwave figures of merits are explained as follows.

The f_T for a bipolar device is given by [19]

$$f_T = \frac{1}{2\pi\tau_{EC}} = \frac{1}{2\pi(\tau_E + \tau_B + \tau_C + \tau_{CC})}, \quad (2-14)$$

where τ_{EC} is the total delay time (or emitter-to-collector transit time), τ_E the emitter charging time, and τ_{CC} the collector charging time. The τ_E and τ_{CC} are delay times due to parasitic elements written by

$$\tau_E = \left(\frac{kT}{qI_E} \right) \cdot (C_{EB} + C_{BC}) \cong \left(\frac{kT}{qI_C} \right) \cdot (C_{EB} + C_{BC}), \quad (2-15)$$

and

$$\tau_{CC} = (R_{EE} + R_C) \cdot C_{BC}, \quad (2-16)$$

where C_{EB} is the emitter-base junction capacitance, C_{BC} the base-collector junction capacitance, R_{EE} the emitter resistance, and R_C the collector resistance. It is found that large collector current operation is essential to reduce τ_E . However, the large current increases the power consumption. Therefore, the reduction of C_{EB} and C_{BC} , that is, the scaling down of the device dimension, is inevitable for the high-speed and low-power operation. The small C_{BC} is also effective to reduce τ_{CC} . For the reduction of τ_{CC} , the reduction of parasitic resistance is also important.

The τ_B is the transit time for electrons traveling through the quasi-neutral base region. When electron transport is diffusive, τ_B is given by [9]

$$\tau_B = \frac{W_B^2}{\eta D_n}, \quad (2-17)$$

where W_B is the thickness of the base layer, and η is the adjusting factor for the possible built-in electric field in the base region. Here η is 2 when a uniform base is used. In a very thin base, in contrast, insufficient scattering of electrons makes the transport nonequilibrium [20,21], and τ_B is expressed as [22]

$$\tau_B = \frac{W_B}{v_B}, \quad (2-18)$$

where v_B is the mean velocity of electrons in the base. These equations indicate that the base layer must be thinned to reduce the base transit time.

The τ_C is the transit time for electrons traveling through the base-collector depletion region and is given approximately by [23]

$$\tau_C = \int_0^{W_{BCi}} \frac{1}{v(x)} \left(1 - \frac{x}{W_{BCi}} \right) dx \cong \frac{W_{BCi}}{2v_{sat}}, \quad (2-19)$$

where W_{BCi} is the width of the intrinsic base-collector depletion region, and v_{sat} is the electron saturation velocity. It should be noted that, in III-V devices, the velocity of carriers tends to overshoot the steady-state saturation velocity at the base side of the base-collector depletion region [24,25], so the true τ_C may be smaller than that estimated by this equation. Equation (2-19) implies that τ_C can be significantly reduced when the W_{BCi} is designed to be very thin. However, the thin W_{BCi} not only degrades the breakdown voltage, but also increases C_{BC} , which limits the f_T improvement because of the increase in both τ_E and τ_{CC} . Therefore, a moderate thickness is required for W_{BCi} .

The other figure-of-merit, f_{max} , is limited by the charging time of the input and output RC networks of a transistor. The f_{max} is given by [26,27]

$$f_{max} = \sqrt{\frac{f_T}{8\pi R_B C_{BC}}}, \quad (2-20)$$

where R_B is the base resistance. This equation means that high f_T , small R_B , and small C_{BC} result in high f_{max} . Since small C_{BC} also results in high f_T , as stated previously, the reduction in C_{BC} is indispensable for achieving excellent high-frequency performance in HBTs. In determining the f_{max} , Mason's unilateral power gain U is widely used for the extrapolation because U does not vary if the transistor is embedded in a lossless reciprocal network [28]. Other commonly quoted power gains include the maximum available power gain (MAG), relevant for those frequencies where the device is unconditionally stable, and the maximum stable power gain (MSG), relevant for those frequencies where the device is potentially unstable [29].

2.3 Characteristics of Conventional InGaP/GaAs HBTs

In order to understand the fundamental characteristics of InGaP/GaAs HBTs, devices with a conventional structure were fabricated and evaluated. The characteristics were analyzed to reveal the issues to be solved for high-speed and low-power operations of InGaP/GaAs HBTs.

2.3.1 Device structure and fabrication process

The epitaxial layers of the fabricated InGaP/GaAs HBTs were grown on semi-insulating GaAs (100) substrates by gas-source molecular beam epitaxy [30]. The group III sources were elemental Ga and In, and the group V sources were thermally cracked arsine (AsH_3) and phosphine (PH_3). The n - and p -type dopants were Si and C, respectively. Carbon-tetrabromide (CBr_4) was used as the carbon source. CBr_4 was supplied without a carrier gas by using a closed-loop pressure-control system consisting of a pressure gauge and a control valve. The parameters of the epitaxial layer structure are listed in Table 2-1. Triple emitter-cap layers were used in order to reduce the emitter resistance: 50-nm-thick InGaAs doped to $4 \times 10^{19} \text{ cm}^{-3}$, 50-nm-thick GaAs doped to $5 \times 10^{18} \text{ cm}^{-3}$, and 50-nm-thick InGaP doped to $8 \times 10^{18} \text{ cm}^{-3}$. The InGaP emitter layer was 50 nm thick and doped to $1 \times 10^{18} \text{ cm}^{-3}$. The base layer was 30 nm thick and doped to $1 \times 10^{20} \text{ cm}^{-3}$. The collector layer consisted of 200-nm-thick undoped GaAs. The thick GaAs subcollector (800 nm, $5 \times 10^{18} \text{ cm}^{-3}$) was used to reduce the collector resistance. HBTs with the base thickness of 50 nm were also fabricated in order to investigate its influence on the high-frequency performance.

Conventional mesa structure devices were fabricated by using selective wet chemical etching and a standard photolithographic process. The main steps in the fabrication process are shown in Fig. 2-3. First, WSi is deposited on the InGaAs cap layer as a non-alloyed emitter electrode. The emitter electrode is defined by electron cyclotron resonance (ECR) plasma etching (Fig. 2-3(a)). This is followed by the formation of an emitter mesa by wet chemical etching using the emitter electrode as a mask. The InGaAs and GaAs layers are

Table 2-1. Parameters of epitaxial layer structure of fabricated HBTs.

Layer	Material	Doping Concentration (cm ⁻³)	Thickness (nm)
Emitter-cap	<i>n</i> -InGaAs	4×10^{19}	50
	<i>n</i> -GaAs	5×10^{18}	50
	<i>n</i> -InGaP	8×10^{18}	50
Emitter	<i>n</i> -InGaP	1×10^{18}	50
Base	<i>p</i> -GaAs	1×10^{20}	30
Collector	un-GaAs	undoped	200
Subcollector	<i>n</i> -GaAs	5×10^{18}	800

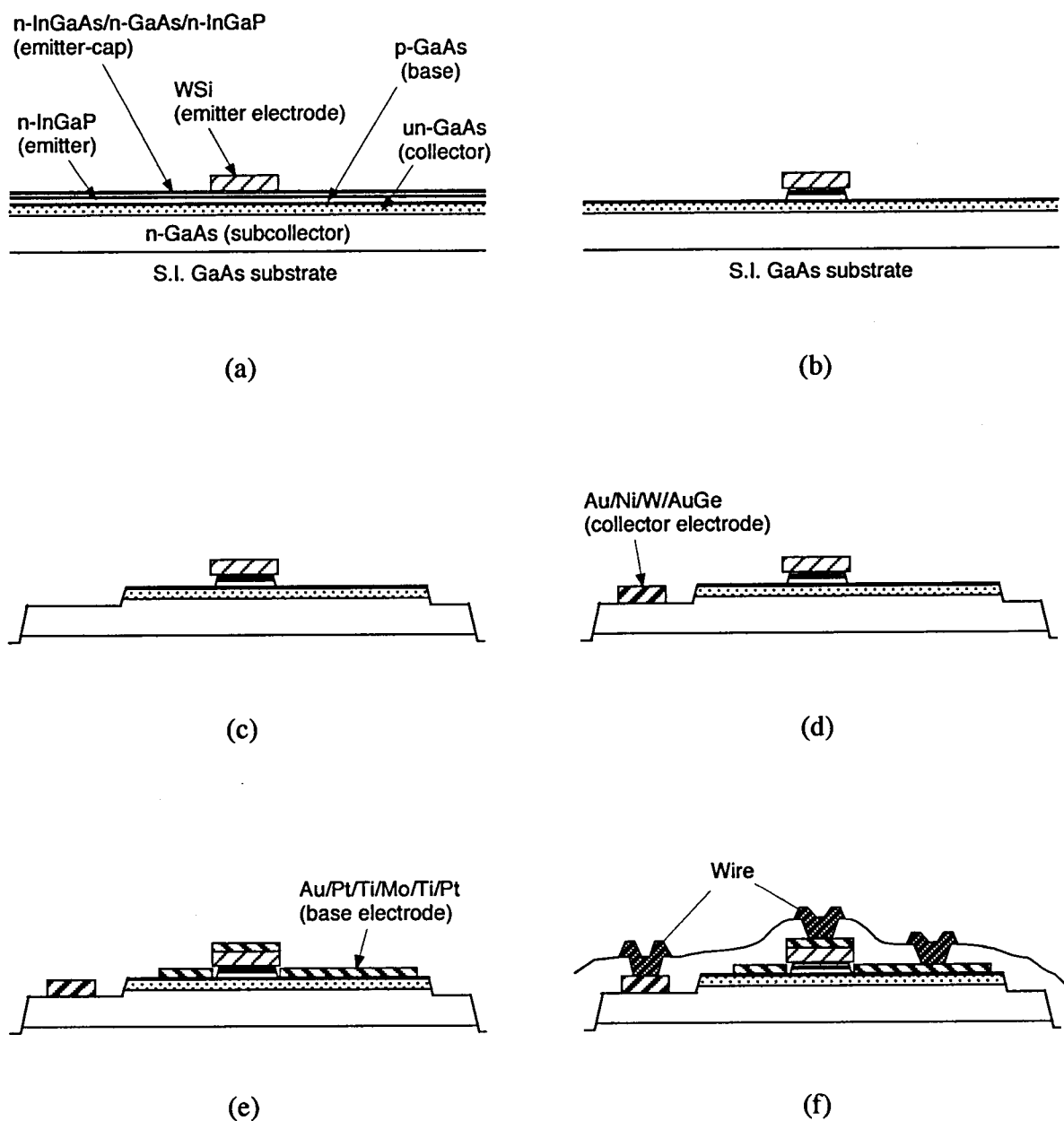


Fig. 2-3. Main steps in the schematic fabrication process of conventional HBTs.

etched selectively with $\text{H}_3\text{PO}_4\text{:H}_2\text{O}_2\text{:H}_2\text{O}$, and the InGaP layer is etched selectively by a solution of dilute HCl (Fig. 2-3(b)). Then, the base-collector and isolation mesas are formed by wet chemical etching using photoresist as an etching mask (Fig. 2-3(c)). Au/Ni/W/AuGe metals are evaporated on the subcollector as a collector electrode. They are lifted off, and then alloyed at 350°C for 30 min (Fig. 2-3(d)). Au/Pt/Ti/Mo/Ti/Pt metals are deposited on the base layer and lifted off as a non-alloyed base electrode. Here, the emitter and the base electrode are separated in a “conventional” self-aligned manner: i.e., side etching of the emitter is used to form the spacing between the emitter and the base electrode. Since the self-aligned process was already used in the development of the first AlGaAs/GaAs HBTs reported in 1972 [31], the process is called as “conventional” in this thesis. The extrinsic base surface does not have a ledge passivation (Fig. 2-3(e)). The devices are then passivated with SiO_2 by photo-assisted chemical vapor deposition at a substrate temperature of 300°C . Finally, the metallization process follows and the device structure is completed (Fig. 2-3(f)).

2.3.2 DC characteristics

A typical Gummel plot of the fabricated conventional HBT with an emitter size of $1.2\ \mu\text{m} \times 3.4\ \mu\text{m}$ is shown in Fig. 2-4. The collector current exhibits exponential behavior with an ideality factor of 1.0. The turn-on voltage V_{on} measured at a collector current density J_C of $1\ \text{A}/\text{cm}^2$ is about 1.1 V. This value is almost the same as that in AlGaAs/GaAs HBTs with a graded heterojunction [32-34], suggesting that ΔE_C of the InGaP/GaAs heterojunction is relatively small; i.e., collector currents of InGaP/GaAs HBTs can be expressed by Eq. (2-4). In contrast, the V_{on} of AlGaAs/GaAs HBTs with an abrupt heterojunction is about 1.3 V [10,32,33]. This result verifies that InGaP/GaAs is a useful material system for keeping the low V_{on} of GaAs HBTs without using a graded heterojunction. The ideality factor of the base current, on the other hand, is 2.0 at low bias voltage, suggesting that the base current mainly originates from recombination at the emitter-base depletion region. The ideality factor becomes smaller at higher bias voltage and, as a result, the maximum current gain of 40 is obtained at a collector current density of $2.5 \times 10^5\ \text{A}/\text{cm}^2$.

In order to investigate the emitter size effect of InGaP/GaAs HBTs, the dependence of

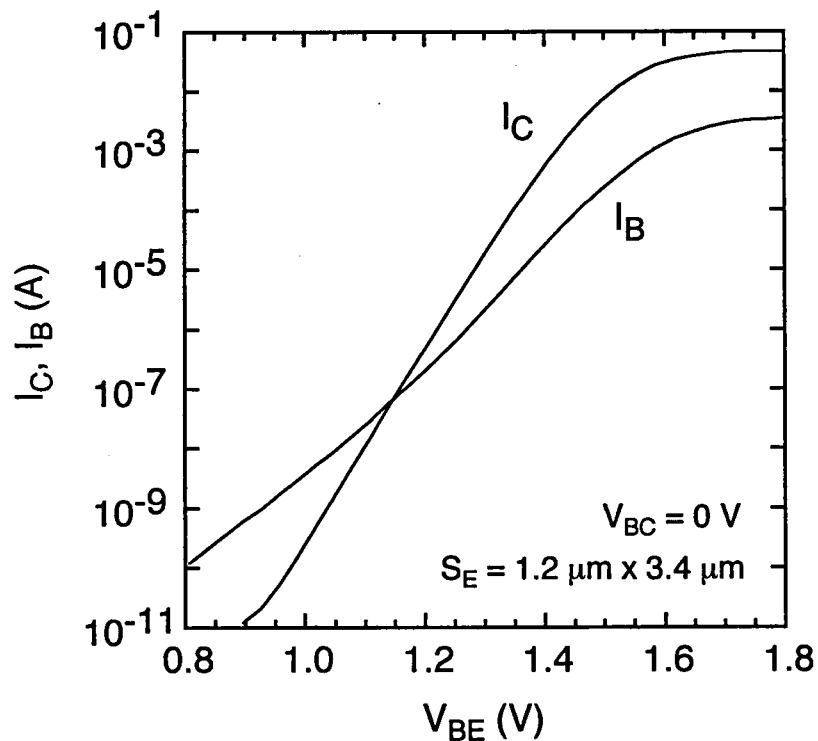


Fig. 2-4. Gummel plot of the fabricated HBT with an emitter size of $1.2 \mu\text{m} \times 3.4 \mu\text{m}$.

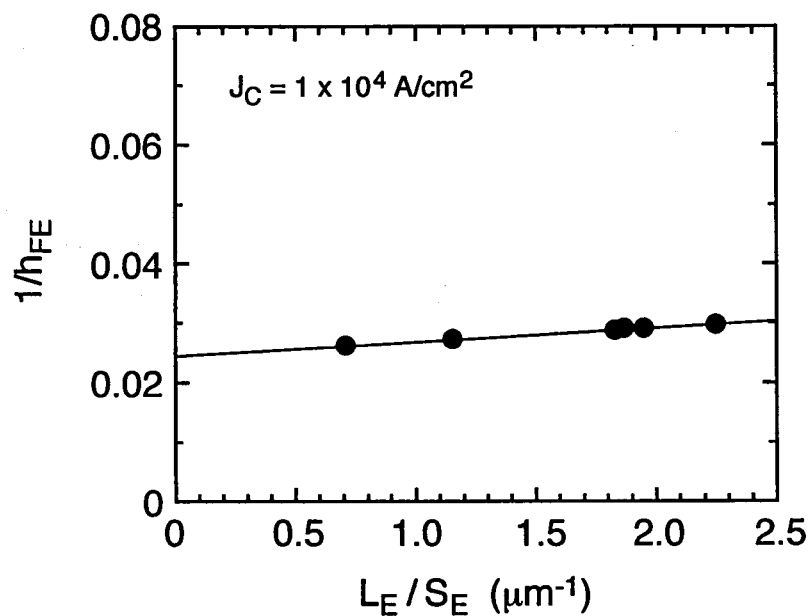


Fig. 2-5. $1/h_{FE}$ versus L_E/S_E for the fabricated HBTs at $J_C = 1 \times 10^4 \text{ A/cm}^2$.

the current gain h_{FE} on the emitter size S_E was evaluated. The dependence is based on the relationship approximately expressed as [35]

$$\frac{1}{h_{FE}} = \frac{1}{h_{FEi}} + \frac{J_{Bp}}{J_C} \cdot \frac{L_E}{S_E}, \quad (2-21)$$

where h_{FEi} is the intrinsic current gain explained by the Eqs. (2-8) – (2-11), J_{Bp} the base current density due to peripheral recombination, J_C the collector current density, and L_E the length of the emitter periphery. Figure 2-5 shows the dependence of $1/h_{FE}$ on L_E/S_E for the fabricated HBTs at a collector current density of 1×10^4 A/cm². This plot distinguishes between the intrinsic base current and the surface recombination current around the emitter periphery. From the slope of the line in Fig. 2-5, the peripheral component of the base current was estimated to be 2.3×10^{-7} A/ μ m. The value is comparable to that of AlGaAs/GaAs HBTs with an AlGaAs surface passivation layer [36], although the extrinsic base regions of the fabricated HBTs do not have passivated by thin emitter layers. This result indicates that the InGaP emitter effectively suppresses the emitter size effect of GaAs HBTs. The small peripheral current is probably attributed to the lower surface recombination velocity and lower deep level density of InGaP than those of AlGaAs [37]. Using the relatively thin base layer is another possible cause, since the thin base reduces the lateral diffusion of electrons and, thus, suppresses the electron injection into the extrinsic base region [35,38].

2.3.3 High-frequency characteristics

The high-frequency characteristics of the fabricated conventional InGaP/GaAs HBTs were evaluated by on-wafer s -parameter measurements in the frequency range from 100 MHz to 25.1 GHz. The pad parasitics were de-embedded by using the method presented by Costa et al. [39]. The f_T and f_{max} were estimated from -20dB/decade extrapolations of the frequency dependence of small-signal current gain $|h_{21}|^2$ and Mason's unilateral gain U [9,18].

Figure 2-6 shows the dependence of $|h_{21}|^2$ and U on frequency of an HBT with an emitter size of $1.2 \mu\text{m} \times 3.4 \mu\text{m}$. At the collector-emitter voltage of 1.6 V, a peak f_T of 115 GHz and a peak f_{max} of 159 GHz were achieved. Figure 2-7 shows the f_T and f_{max} as a function of

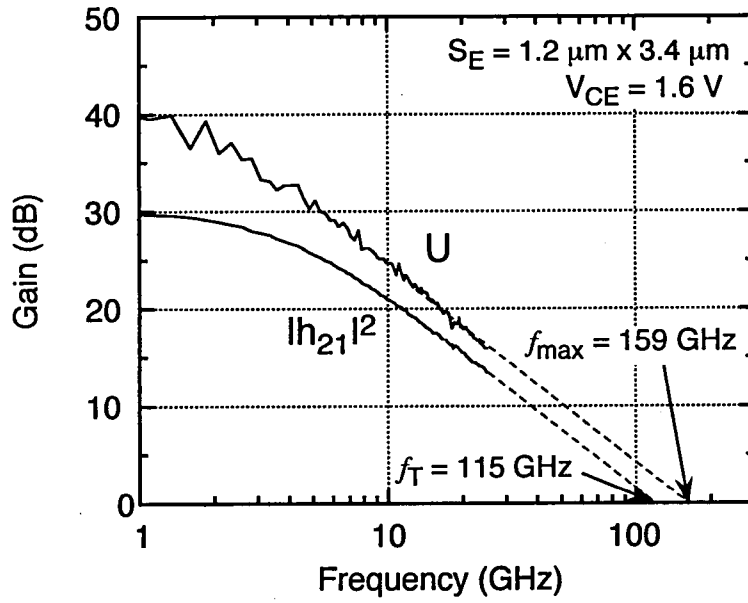


Fig. 2-6. $|h_{21}|^2$ and U as a function of frequency of fabricated HBT. The dashed lines are extrapolations of $|h_{21}|^2$ and U with a -20dB/decade slope.

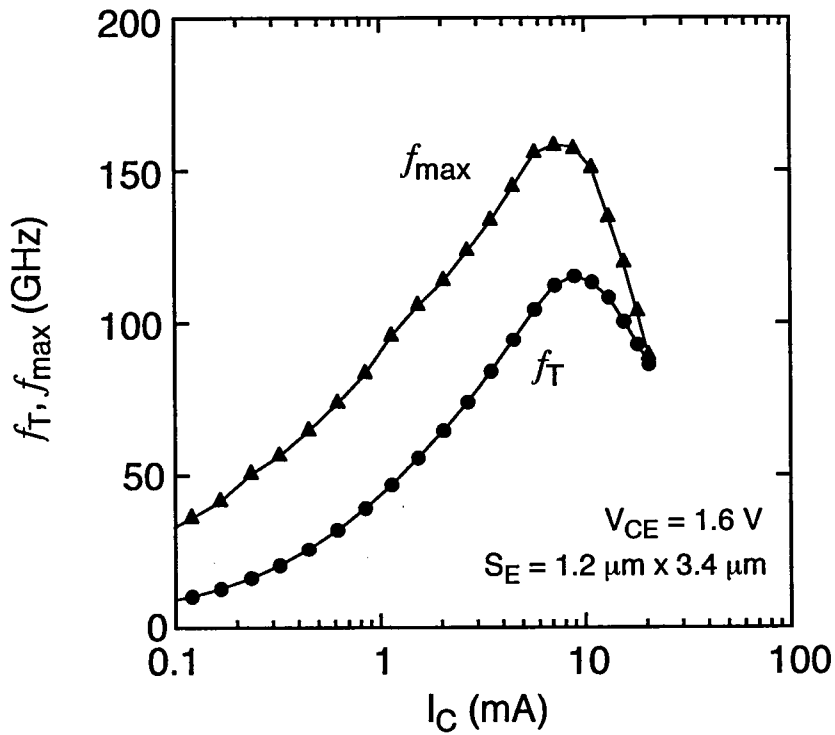


Fig. 2-7. Dependence of f_T and f_{max} on the collector current of the fabricated HBT at $V_{CE} = 1.6 \text{ V}$.

collector current. The peak f_T and f_{\max} were obtained at a collector current of 8 mA, at which a collector current density of about 2×10^5 A/cm². The characteristics of the HBT are summarized in Table 2-2. The emitter resistance R_{EE} was measured by an open-collector method [40] and the collector resistance R_C was estimated from the results of transmission line model (TLM) measurements [41,42]. The emitter-base capacitance C_{EB} and the base-collector capacitance C_{BC} were calculated from the measured s -parameters at 5 GHz.

The delay time analysis was carried out by using these results. As stated in the previous section, total delay time τ_{EC} is approximately expressed by using the Eqs. (2-14) – (2-16) as

$$\tau_{EC} = 1/2\pi f_T = kT/qI_C (C_{EB} + C_{BC}) + \tau_B + \tau_C + (R_{EE} + R_C)C_{BC}. \quad (2-22)$$

This equation indicates that the $\tau_E (= kT/qI_C (C_{EB} + C_{BC}))$ is estimated by extrapolating the $1/(2\pi f_T)$ versus $1/I_C$ curve to $1/I_C = 0$. Figure 2-8 shows the plot of total delay time as a function of inverse collector current. The τ_E was estimated to be 0.35 ps from this figure. The τ_{CC} calculated by R_{EE} , R_C , and C_{BC} listed in Table 2-2 was 0.38 ps. As a result, the intrinsic transit time, $\tau_F (= \tau_B + \tau_C)$, was calculated to be 0.65 ps. Figure 2-9 shows the comparison of delay time in HBTs with the base thickness of 30 nm and 50 nm. The τ_F of HBTs with 50-nm base was estimated to be 1.05 ps; about 40% reduction in τ_F can be achieved by reducing the base thickness from 50 nm to 30 nm. This result suggests that the intrinsic transit time can be effectively reduced by decreasing the base thickness.

Figure 2-10 shows the dependence of delay time on the emitter size of fabricated HBTs at a collector current density of 1×10^5 A/cm². Since the τ_F is determined by the thickness of the neutral base and the collector depletion region, τ_F is constant for all sizes of devices. In contrast, both τ_E and τ_{CC} increase as the emitter size is reduced, and become the dominant factors in the total delay time of small devices. This result indicates that the reduction of parasitic delay times by reducing the parasitic resistance and capacitance is especially important for the high-speed operation of small-scale HBTs.

Table 2-2. Device characteristics of the fabricated HBT.

Emitter Size	1.2 μm x 3.4 μm	
$h_{FE\text{max}}$	40	
BV_{CBO}	9.8	V
BV_{CEO}	11.0	V
R_{EE}	6.6	Ω
R_B	25	Ω
R_C	8.1	Ω
C_{EB}	13.8	fF
C_{BC}	25.8	fF
f_T	115	GHz
f_{max}	159	GHz

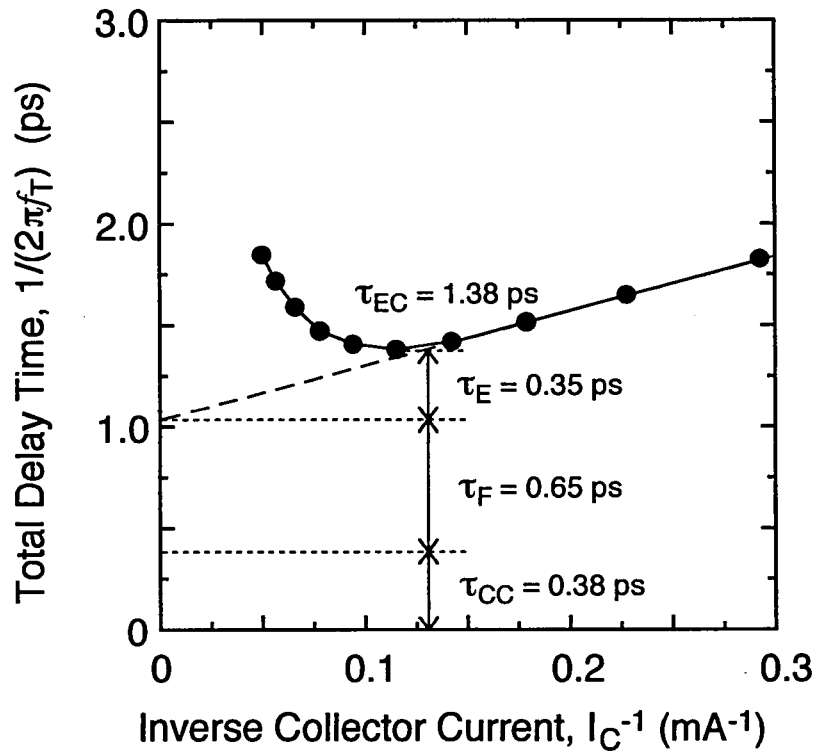


Fig. 2-8. Plot of total delay time against inverse collector current of the fabricated HBT.

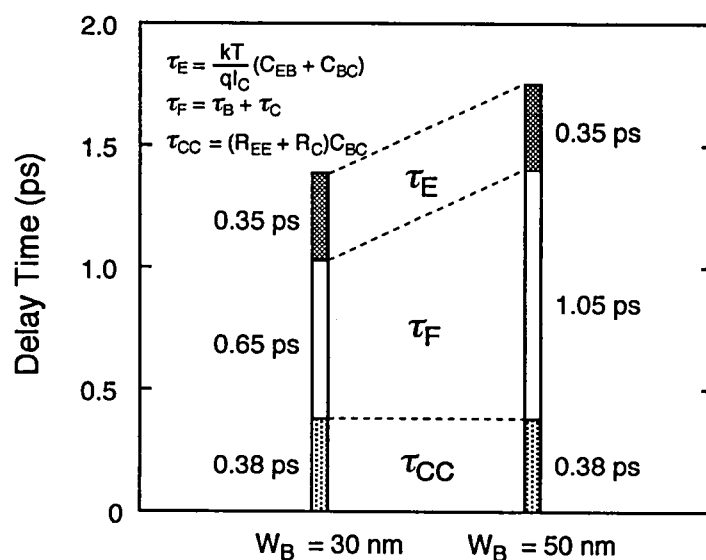


Fig. 2-9. Comparison of total delay time in HBTs with the base thickness of 30 nm and 50 nm.

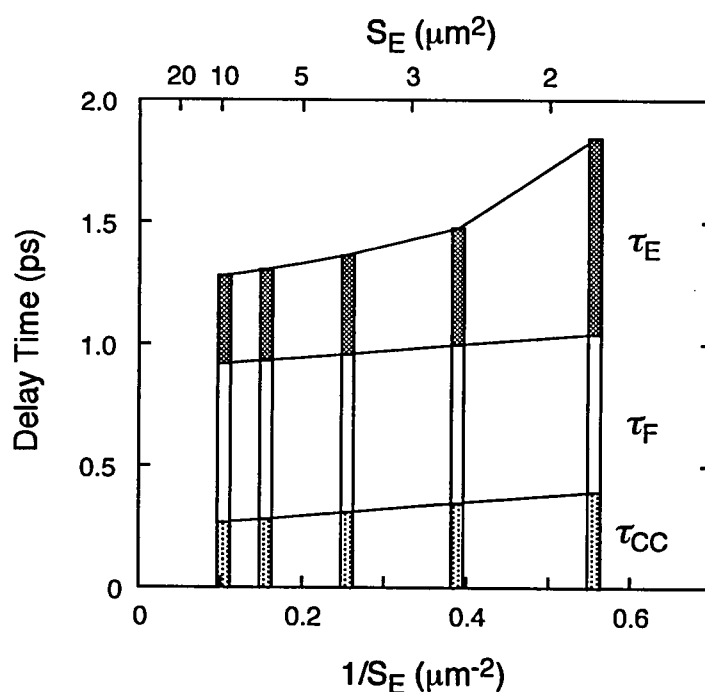


Fig. 2-10. Dependence of delay time on emitter size of fabricated HBTs at a collector current density of $1 \times 10^5 \text{ A/cm}^2$.

2.4 Guides to High-Speed and Low-Power Operations

For the high-speed operation of GaAs HBTs, the most struggling issue is the reduction of the intrinsic transit time τ_F . This is because the τ_F occupies about the half of the total delay time, as shown in Fig. 2-9. In addition, the τ_F is larger than that of InP HBTs [43]. To reduce the τ_F , reducing the vertical scale of the epitaxial layers is indispensable, as expressed in Eqs. (2-17) – (2-19). However, thinning the collector layer gives rise to the increase of the base-collector capacitance, which adversely affects the increase of the parasitic delay time, as well as the degradation to the breakdown voltage. Therefore, vertical scaling of the collector layer is not preferable. In contrast, thinning the base layer effectively reduces the τ_F without sacrificing any delay time, as shown in Fig. 2-9. Although the thin base layer suffers from the increase in the base resistance and thus degrades f_{\max} , the degradation can be suppressed by increasing the base doping level. However, the highly doped base, in turn, increases the back injection of holes or reduces the diffusion length of electrons in the base, both of which reduce the current gain, as expressed in Eq. (2-7) or Eq. (2-8). Therefore, the thickness and the doping concentration of the base layer must be optimized by considering the trade-off relationship between the current gain, the base transit time, and the base resistance.

Another issue for the high-speed operation is the suppression of the increase in the parasitic delay time when scaling down the device dimension for the low-power operation. The main reason can be explained by Fig. 2-11. Figure 2-11 shows schematic cross-sections of conventional HBTs with an emitter width of (a) 2 μm and (b) 0.5 μm . A certain amount of the extrinsic base-collector junction area is needed as the contact pad region to contact the base electrode and the wire. Since this area cannot be scaled down, the extrinsic collector region relatively increases when scaling down the emitter size, as shown in Fig. 2-11. This becomes the large parasitic component of the base-collector capacitance and, thus, increases both τ_E and τ_{CC} , as expressed in Eqs. (2-15) and (2-16). To improve the high-frequency performance of small-scale HBTs, therefore, the parasitic capacitance originating from the extrinsic collector should be simultaneously reduced with the emitter size.

For the low-power operation of GaAs HBTs, in contrast, the issue is the reduction of the

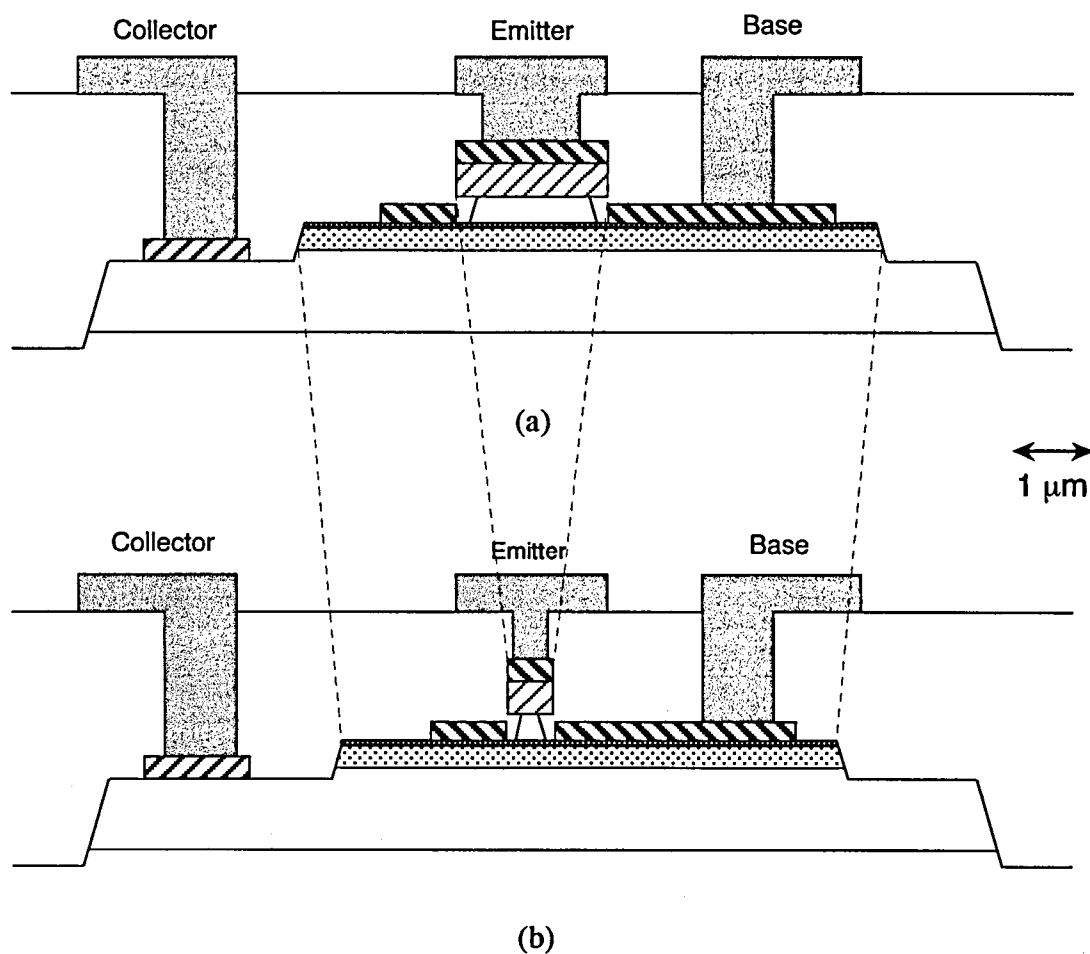


Fig. 2-11. Schematic cross-sections of conventional HBTs with an emitter width of (a) $2\ \mu\text{m}$ and (b) $0.5\ \mu\text{m}$.

turn-on voltage V_{on} . As expressed in Eqs. (2-3) – (2-5), small ΔE_C or graded heterojunction as well as narrow bandgap base is necessary to reduce V_{on} . Since the ΔE_C of InGaP/GaAs heterojunction is relatively small, the InGaP/GaAs HBTs exhibited smaller V_{on} than abrupt AlGaAs/GaAs HBTs. However, due to the large bandgap of GaAs used as the base layer, the V_{on} is still larger than those of InP and SiGe HBTs. Hence, the development of narrow bandgap materials for the base layer is inevitable to reduce the turn-on voltage of GaAs HBTs.

2.5 Summary

Device physics and figures-of-merits of HBTs were reviewed to understand the correlations between material properties, device designs, and device characteristics. The characteristics of conventional InGaP/GaAs HBTs were evaluated and analyzed in detail in order to exploit InGaP/GaAs HBTs for use in high-speed and low-power applications.

The V_{on} of abrupt InGaP/GaAs HBTs was almost the same as that in AlGaAs/GaAs HBTs with a graded heterojunction. This result suggests that ΔE_C between InGaP/GaAs heterointerface was extremely small; namely, InGaP/GaAs is a useful material system for keeping the low V_{on} of GaAs HBTs without using a graded heterojunction. However, the V_{on} was still larger than those of InP and SiGe HBTs because of the large bandgap of GaAs used as the base layer. The peripheral base current of InGaP/GaAs HBTs without surface passivation was comparable to that of AlGaAs/GaAs HBTs with surface passivation. This result indicates that the lower surface recombination velocity of InGaP than those of AlGaAs effectively suppresses the emitter size effect.

The delay time analysis showed that the main component of the delay was the intrinsic delay time τ_F . The τ_F effectively decreased by reducing the base thickness, though the thin base suffers from the increase in the base resistance. The dependence of delay time on the emitter size exhibited that the dominant factors in the total delay time of small devices were parasitic delays, τ_E and τ_{CC} . The delays increased as the emitter size was scaled down because the extrinsic collector region to contact the base electrode and the wire was not scaled down.

Based on the above results, the guides for high-speed and low-power operation of GaAs HBTs were concluded as follows:

- To improve both f_T , and f_{\max} , the design of the base layer, i.e., the doping concentration and the thickness, should be optimized by considering the trade-off relationship between the current gain, the base transit time, and the base resistance;
- To improve the high-frequency performance of small-scale HBTs, the parasitic base-collector capacitance should be reduced simultaneously as the emitter size is scaled down;
- To reduce V_{on} of GaAs HBTs, narrow bandgap materials for the base layer must be developed.

The detail methods to solve these issues are discussed and demonstrated in the following chapters. The optimum design of the base layer related to the base concentration and thickness are discussed in chapter 3. For the simultaneous reduction of the emitter size and the parasitic capacitance, a novel device structure aimed at physically removing GaAs in the extrinsic collector is proposed in chapter 4. The capability of the novel structure devices for high-speed and low-power ICs is investigated in chapter 5. For the reduction of the turn-on voltage, GaAs HBTs with a pseudomorphic GaAsSb as the narrow-bandgap base layer are demonstrated in chapter 6.

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Chapter 3

Characterization of InGaP/GaAs HBTs with Heavily-Doped and Thin Base

3.1 Introduction

As discussed in chapter 2, optimization of the base layer design is essential to improve the high-frequency performance of HBTs. Using a thin base layer reduces base transit time, which improves a cutoff frequency, f_T , but it simultaneously increases the base resistance, which adversely degrades a maximum oscillation frequency, f_{max} . To keep the base sheet resistance low for the thin base, an extremely high base doping is required. However, the heavily-doped base leads to the reduction of the current gain resulting from the increase of both the back injection of holes into the emitter and the recombination in the neutral base region.

In order to optimize the base doping concentration and the thickness, therefore, it is important to understand their influences on both DC and high-frequency characteristics. With regard to the base doping concentration, the relations with current gain at the base doping level below $1 \times 10^{20} \text{ cm}^{-3}$ have already been examined [1-4]. However, the relations for InGaP/GaAs HBTs with extremely high base concentrations above $1 \times 10^{20} \text{ cm}^{-3}$ have not been fully investigated [5,6]. With respect to the base thickness, on the other hand, the relations

with base transit time in AlGaAs/GaAs HBTs have been estimated by simulations [7,8]. However, the transit time on InGaP/GaAs HBTs has not been investigated in detail so far.

In response to the above situations, the characteristics of InGaP/GaAs HBTs with a heavily-doped and thin base are studied in this chapter. The dependence of the current gain on the base doping concentration are evaluated at the doping level ranging from 5×10^{19} to $5 \times 10^{20} \text{ cm}^{-3}$. The results are analyzed in detail to reveal what is the dominant factor to determine the current gain at the extremely high doping. On the other hand, the influences of the base thickness W_B on DC and high-frequency characteristics are examined at W_B ranging from 15 to 80 nm. The base transit time is estimated from the current gain and the intrinsic transit time. Based on the results, design of the optimum base layer is discussed.

3.2 Experimental Procedures

The epitaxial layers were grown on semi-insulating GaAs (100) substrates by gas-source molecular beam epitaxy (GSMBE), the details of which are described in chapter 2. The p -type dopant is carbon, which is favorable to obtain heavily-doped and thin p -GaAs layers because of its low diffusion coefficient compared with other p -type dopants [9]; so it can produce an abrupt p - n junction even at higher doping levels, i.e., over $1 \times 10^{20} \text{ cm}^{-3}$ [10-12]. The parameters of the epitaxial layer structure are listed in Table 3-1. In order to investigate the effects of the base concentration N_B , HBT epitaxial layers with N_B ranging from 5×10^{19} to $5 \times 10^{20} \text{ cm}^{-3}$ were prepared, where the base thickness was fixed to 30 nm. On the other hand, in order to investigate the influences of the base thickness W_B , epitaxial layers with W_B ranging from 15 to 80 nm were prepared. In this case, the base doping level was fixed to $1 \times 10^{20} \text{ cm}^{-3}$.

For analyzing DC characteristics, conventional mesa structure devices were utilized. For analyzing high-frequency performance, in contrast, self-aligned mesa structure devices were fabricated. A schematic cross-section of the self-aligned HBT is shown in Fig. 3-1. In addition to the self-aligned emitter-base formation, as described in chapter 2, the base and the collector mesas were etched by using the base electrode as an etching mask [13]. The

Table 3-1. Parameters of epitaxial layer structure of fabricated InGaP/GaAs HBTs.

Layer	Material	Doping Concentration (cm^{-3})	Thickness (nm)
Emitter-cap	<i>n</i> -InGaAs	4×10^{19}	50
	<i>n</i> -GaAs	8×10^{18}	100
	<i>n</i> -InGaP	8×10^{18}	50
Emitter	<i>n</i> -InGaP	5×10^{17}	100
Base	<i>p</i> -GaAs	N_B	W_B
Collector	<i>n</i> -GaAs	2×10^{16}	200
Subcollector	<i>n</i> -GaAs	8×10^{18}	800

N_B : $5 \times 10^{19} \sim 5 \times 10^{20}$

W_B : 15 ~ 80

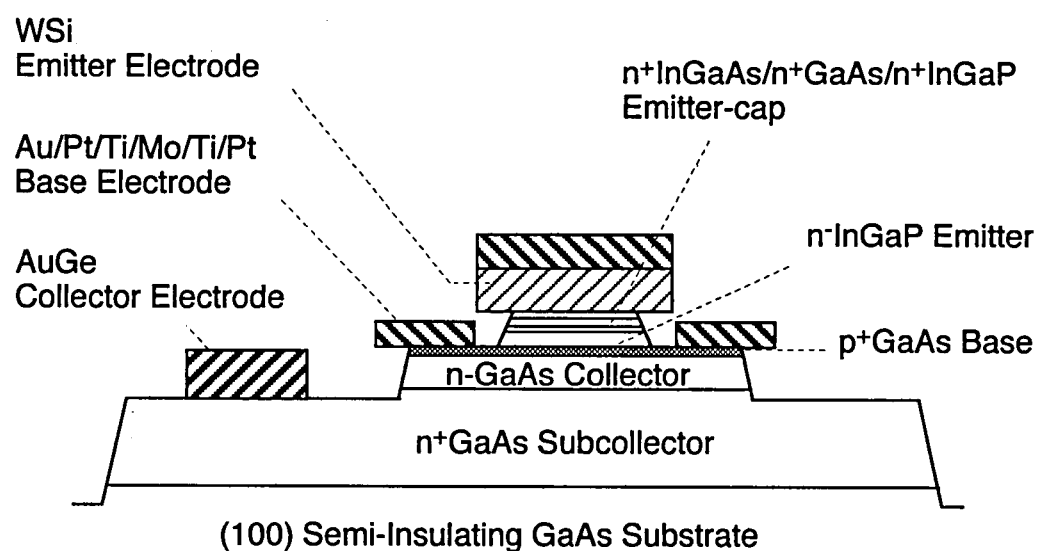


Fig. 3-1. Schematic cross-section of self-aligned HBT.

side etching under the base electrode reduces the base-collector capacitance and, thus, decreases the parasitic delay time. High-frequency characteristics were evaluated by on-wafer s -parameter measurements in the frequency range of 100 MHz – 40 GHz.

3.3 Effects of Base Doping Concentration

3.3.1 Experimental results

To investigate the bulk quality of the base layers with heavily carbon doping, the properties of holes as the majority carrier were evaluated. Figure 3-2 shows the dependence of hole mobility on carrier concentration N_B in p -GaAs. The concentrations were evaluated by Hall measurements using a van der Pauw configuration. At N_B of up to $4 \times 10^{20} \text{ cm}^{-3}$, the mobility gradually decreases in inverse proportion to $N_B^{1/3}$; this result is consistent with the theoretical calculation by Walukiewicz [14]. At higher N_B , however, the mobility drastically decreases as the carrier concentration increases. Ouchi et al. revealed by X-ray diffractions that the p -GaAs grown by the GSMBE system utilized in this study had non-activated or compensating C atoms at the As or Ga lattice sites when the doping concentration was above $4.6 \times 10^{20} \text{ cm}^{-3}$ [15]. Therefore, the drastic decrease in the hole mobility is probably caused by the reduction of the activation rate of C. Since the decrease in the hole mobility limits the reduction in sheet resistance of heavily-doped base layers, characteristics of HBTs with N_B of less than $4.6 \times 10^{20} \text{ cm}^{-3}$ were evaluated hereafter.

Typical Gummel plots for HBTs with N_B of $1 \times 10^{20} \text{ cm}^{-3}$ and $4 \times 10^{20} \text{ cm}^{-3}$ are shown in Fig. 3-3. The emitter size of the measured devices was $10 \mu\text{m} \times 10 \mu\text{m}$. The ideality factor of the collector current I_C in both devices is 1.0. On the other hand, the ideality factor of the base current n_B at low base-emitter bias voltage V_{BE} is 2.0 in both devices, and at high V_{BE} , n_B is about 1.1 for N_B of $1 \times 10^{20} \text{ cm}^{-3}$ and about 1.3 for N_B of $4 \times 10^{20} \text{ cm}^{-3}$. HBTs with N_B of below $3 \times 10^{20} \text{ cm}^{-3}$ have almost the same properties as those shown in Fig. 3-3(a), whereas HBTs with N_B of above $3 \times 10^{20} \text{ cm}^{-3}$ have almost the same properties as those shown in Fig. 3-3(b). The emitter size dependence of the base current showed that the base current with n_B of 2 at low

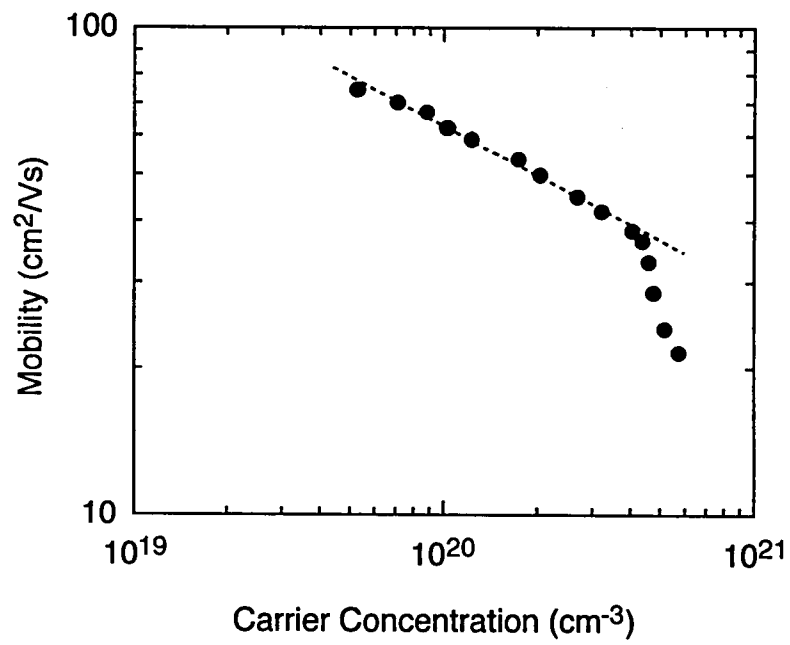
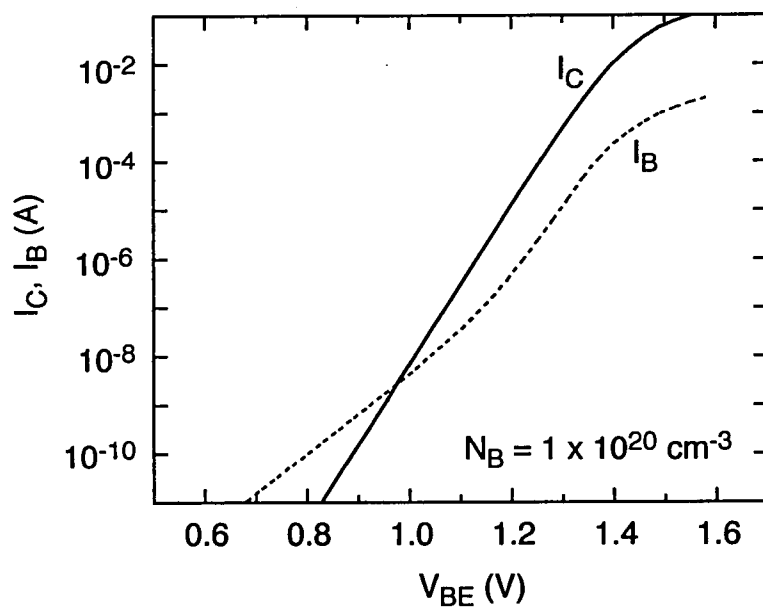
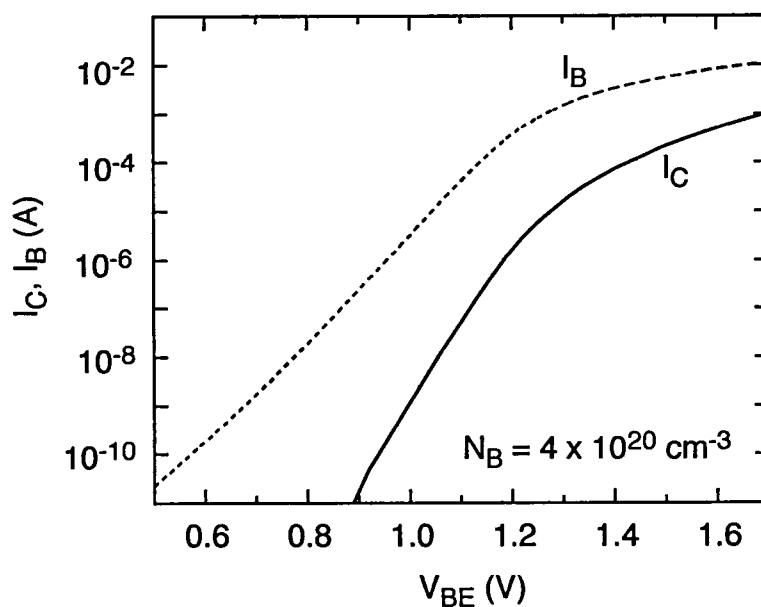


Fig. 3-2. Dependence of hole mobility on carrier concentration in *p*-GaAs.



(a)



(b)

Fig. 3-3. Gummel plots for HBTs with base concentration N_B of (a) $1 \times 10^{20} \text{ cm}^{-3}$ and (b) $4 \times 10^{20} \text{ cm}^{-3}$.

V_{BE} was proportional to the length of the emitter periphery. This indicates that the base current at low V_{BE} originates from the recombination at the emitter depletion region around the emitter periphery. In contrast, the base current with smaller n_B at high V_{BE} was in proportion to the emitter size, suggesting that the contribution of the peripheral base current is insignificant at higher V_{BE} . Figure 3-4 shows the current gain h_{FE} of the HBT with N_B of $1 \times 10^{20} \text{ cm}^{-3}$ as a function of collector current density J_C . The ideality factor of the base current estimated from the slope of the graph is less than 1.2 at J_C above $1 \times 10^2 \text{ A/cm}^2$, suggesting that the recombination current in the emitter depletion region is small enough at the J_C . These results verify that the base current at higher V_{BE} consists of the back-injection current of holes I_{Bh} and the recombination current in the intrinsic bulk base region I_{Bbr} .

Figure 3-5 shows the dependence of h_{FE} on N_B at J_C of $1 \times 10^4 \text{ A/cm}^2$, where the h_{FE} is mainly determined by I_{Bh} and I_{Bbr} . When N_B is less than $3 \times 10^{20} \text{ cm}^{-3}$, the h_{FE} is inversely proportional to the square of N_B . In contrast, the h_{FE} drastically decreases at higher N_B .

3.3.2 Analysis of current gain

Here, the dependence of h_{FE} on N_B shown in Fig. 3-5 was analyzed to clarify their relations. As previously stated, the recombination current in the emitter depletion region can be ignored at the evaluated bias point. Consequently, the current gain h_{FE} can be expressed as

$$h_{FE} = \frac{I_C}{I_B} = \left(\frac{I_{Bh} + I_{Bbr}}{I_C} \right)^{-1} = \left(\frac{1}{h_{FEh}} + \frac{1}{h_{FEbr}} \right)^{-1}, \quad (3-1)$$

where h_{FEh} is the current gain determined by the back injection of holes into the emitter, and h_{FEbr} is the current gain determined by the bulk recombination in the intrinsic base region. Since the conduction band discontinuity ΔE_C at InGaP/GaAs heterojunction is relatively small, as investigated in chapter 2, the h_{FEh} is written as [16,17]

$$h_{FEh} = \frac{L_p D_n N_E n_{iB}^2}{W_B D_p N_B n_{iE}^2} \exp\left(\frac{\Delta E_C}{kT}\right) = \frac{L_p D_n N_E N_{CB} N_{VB}}{W_B D_p N_B N_{CE} N_{VE}} \exp\left(\frac{\Delta E_V}{kT}\right), \quad (3-2)$$

where L_p is the diffusion length of holes in the emitter, W_B the base thickness, D_n and D_p the

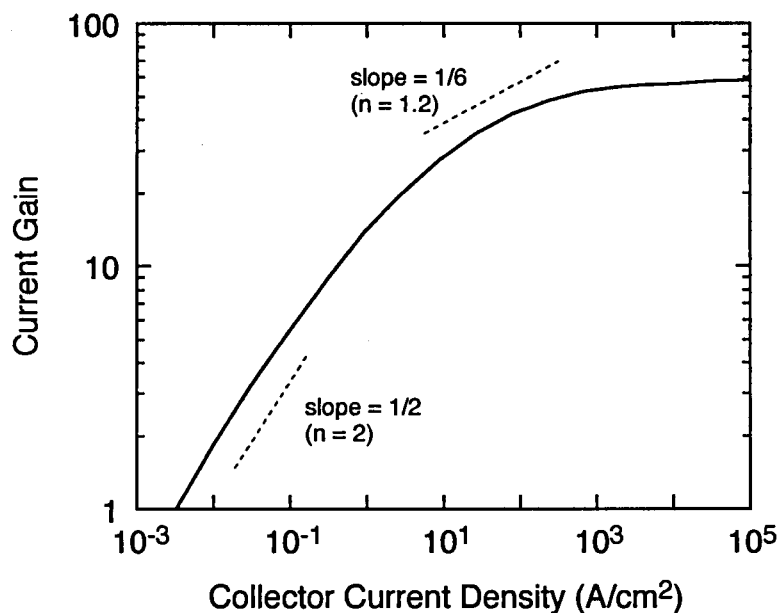


Fig. 3-4. Dependence of current gain h_{FE} on collector current density J_C for HBT with N_B of $1 \times 10^{20} \text{ cm}^{-3}$.

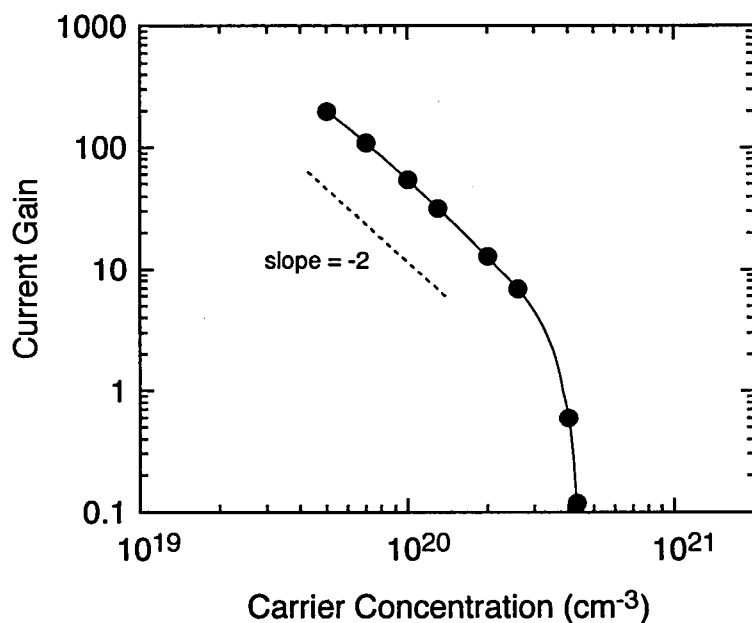


Fig. 3-5. Dependence of current gain h_{FE} on base doping concentration N_B . The gains were measured at J_C of $1 \times 10^4 \text{ A/cm}^2$. The h_{FE} is inversely proportional to the square of N_B when N_B is less than $3 \times 10^{20} \text{ cm}^{-3}$; whereas the h_{FE} drastically decreases at higher N_B .

electron and hole diffusion coefficients, respectively, N_E the emitter doping concentration, n_{iB} and n_{iE} the intrinsic carrier concentrations of base and emitter, respectively, N_{CB} (N_{CE}) and N_{VB} (N_{VE}) the effective densities of states in the conduction and valence bands in the base (emitter), respectively, and ΔE_V the valence band discontinuity. On the other hand, the h_{FEbr} can be written as [17]

$$h_{FEbr} = \frac{1}{\cosh(W_B/L_n) - 1} \approx 2 \cdot \left(\frac{L_n}{W_B} \right)^2 = 2 \cdot \frac{D_n \tau_n}{W_B^2}, \quad (3-3)$$

where L_n is the diffusion length of electrons in the base, and τ_n the minority electron lifetime. The τ_n is given by [18]

$$1/\tau_n = 1/\tau_{SRH,rad} + 1/\tau_A = 1 \times 10^{-10} \cdot N_B + B_A \cdot N_B^2, \quad (3-4)$$

where $\tau_{SRH,rad}$ is the lifetime of Shockley-Read-Hall (SRH) type recombination and radiative recombination, τ_A the lifetime dominated by Auger recombination, and B_A the Auger coefficient.

When N_B is less than $3 \times 10^{20} \text{ cm}^{-3}$, the current gain is inversely proportional to the square of N_B , as shown in Fig. 3-5. Accordingly, the current gain at N_B of less than $3 \times 10^{20} \text{ cm}^{-3}$ can be explained by Auger recombination process in the intrinsic base region. By assuming that the base transit time is 0.2 ps [19], where the diffusion coefficient is calculated to be $23 \text{ cm}^2/\text{s}$, the Auger recombination coefficient was estimated to be $8.1 \times 10^{-30} \text{ cm}^6/\text{s}$, which is in good agreement with the previously reported values ($2 - 10 \times 10^{-30} \text{ cm}^6/\text{s}$) [2,18,20]. When N_B is above $3 \times 10^{20} \text{ cm}^{-3}$, in contrast, the current gain decreases significantly. This result, however, cannot be simply explained only by the dependence on the carrier concentration as aforementioned equations. Since the base current with n_B close to 1 is in proportion to the emitter size at N_B of $4 \times 10^{20} \text{ cm}^{-3}$, it is inferred that the drastic decrease in the current gain by the heavy doping is also ascribed to the increase of the recombination in the neutral base region and the back injection of holes into the emitter.

Regarding the possibility of the significant increase in the bulk recombination, it has been found that the photoluminescence intensity of C-doped GaAs grown by the GSMBE system utilized in this study drastically decreased as the carrier concentration increased [15].

The luminescence disappeared when the carrier concentration exceeded $2 \times 10^{20} \text{ cm}^{-3}$ even though the good majority carrier property was obtained, as shown in Fig. 3-2. This result suggests that the extremely high doping might induce the generation of point defects in the base layer, which reduce the lifetime of recombination and thus increase the bulk recombination in the neutral base region; as a result, the h_{FEbr} is reduced. However, this inference cannot explain that the base current with n_B of 2 at low V_{BE} , which is in proportion to the length of the emitter periphery, also drastically increases at N_B of $4 \times 10^{20} \text{ cm}^{-3}$, as mentioned in the previous paragraph. Hence, the increase in the back injection of holes should be considered to explain the drastic reduction of the current gains at N_B above $3 \times 10^{20} \text{ cm}^{-3}$.

The back injection of holes in HBTs is limited by the barrier height due to the valence band discontinuity ΔE_V , as described in chapter 2. When the base doping level is relatively high, however, the bandgap narrowing and the Fermi level in accordance with the Fermi-Dirac distribution should be taken into consideration for the effective barrier height of holes.

When the base concentration N_B is higher than the N_{VB} , the Fermi energy level E_F is calculated based on the Fermi-Dirac function given by [21]

$$p = N_V F_{1/2} \left(\frac{E_V - E_F}{kT} \right), \quad (3-5)$$

where p is the hole concentration and $F_{1/2}(\eta_f)$ is the Fermi-Dirac integral of order one-half expressed as

$$F_{1/2}(\eta_f) = \frac{2}{\sqrt{\pi}} \int_0^\infty \frac{\eta^{1/2} d\eta}{1 + \exp(\eta - \eta_f)}. \quad (3-6)$$

Figure 3-6 shows the Fermi energies as a function of carrier concentration calculated by the Boltzmann approximation and the Fermi-Dirac integral. As the carrier concentration increases, the Fermi energy level by the Fermi-Dirac function $E_{F(FD)}$ drastically deviates from that by the Boltzmann approximation $E_{F(MB)}$. The ΔE_F in Fig. 3-6 is the difference between $E_{F(FD)}$ and $E_{F(MB)}$, which is written as

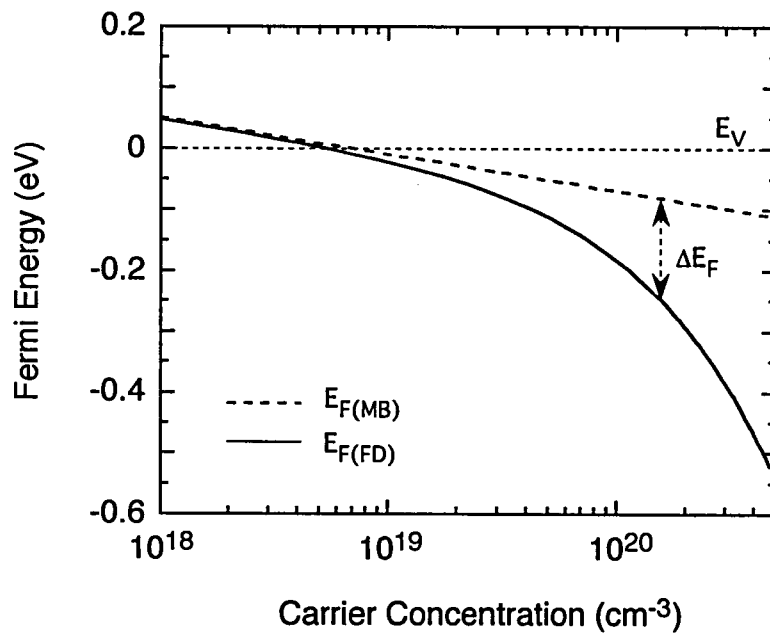


Fig. 3-6. Calculated Fermi energies as a function of carrier concentration. $E_{F(MB)}$ is the result that calculated by the Boltzmann approximation and $E_{F(FD)}$ is the result than calculated by the Fermi-Dirac integral. The dotted line indicates the level of the valence band.

$$\Delta E_F = E_{F(MB)} - E_{F(FD)} = kT \ln \left\{ \frac{\exp[(E_{VB} - E_F)/kT]}{F_{1/2}[(E_{VB} - E_F)/kT]} \right\}. \quad (3-7)$$

In considering Eq. (3-7) and the bandgap narrowing ΔE_{BGN} [17,22], n_{iB}^2/n_{iE}^2 is expressed as

$$\begin{aligned} \frac{n_{iB}^2}{n_{iE}^2} &= \frac{N_{CB} \exp[-(E_{CB} - E_F)/kT] \cdot N_{VB} F_{1/2}[(E_{VB} - E_F)/kT] \cdot \exp(\Delta E_{BGN}/kT)}{N_{CE} \exp[-(E_{CE} - E_F)/kT] \cdot N_{VE} \exp[(E_{VE} - E_F)/kT]} \\ &= \frac{N_{CB} N_{VB}}{N_{CE} N_{VE}} \exp\left(\frac{\Delta E_G + \Delta E_{BGN} - \Delta E_F}{kT}\right), \end{aligned} \quad (3-8)$$

where E_{CB} (E_{CE}) and E_{VB} (E_{VE}) are the conduction and valence band energies of the base (emitter), respectively, and ΔE_G the bandgap difference between the emitter and the base without including ΔE_{BGN} . In consequence, the h_{FEh} given by Eq. (3-2) is finally expressed as

$$h_{FEh} = \frac{L_p D_n N_E N_{CB} N_{VB}}{W_B D_p N_B N_{CE} N_{VE}} \exp\left(\frac{\Delta E_V + \Delta E_{BGN} - \Delta E_F}{kT}\right). \quad (3-9)$$

This indicates that the effective barrier height of holes ΔE_{Veff} ($= \Delta E_V + \Delta E_{BGN} - \Delta E_F$) dominates the h_{FEh} . If the ΔE_F is larger than the ΔE_{BGN} , ΔE_{Veff} becomes smaller than ΔE_V , namely, the back injection of holes into the emitter increases. Hence, the drastic decrease in the current gain at N_B above $3 \times 10^{20} \text{ cm}^{-3}$ is probably explained by considering ΔE_{Veff} .

3.3.3 Effective hole barrier height

To verify the cause of the significant reduction in the current gain at N_B above $3 \times 10^{20} \text{ cm}^{-3}$, the effective hole barrier height ΔE_{Veff} was evaluated from the temperature dependence of current gain. Figure 3-7 shows the typical Arrhenius plots of current gains of HBTs with N_B of 5×10^{19} , 1×10^{20} , and $2 \times 10^{20} \text{ cm}^{-3}$. The data are taken at a J_C of $1 \times 10^4 \text{ A/cm}^2$, where the ideality factor of the base current is almost 1. The junction temperature T_j was determined from the dependence of the current gain on the power consumption and the substrate temperature [23]. At T_j of around 330 K, the $1/h_{FE}$ is almost independent of temperature. The $1/h_{FE}$ is proportional to the square of N_B , indicating that the current gain is dominated by the

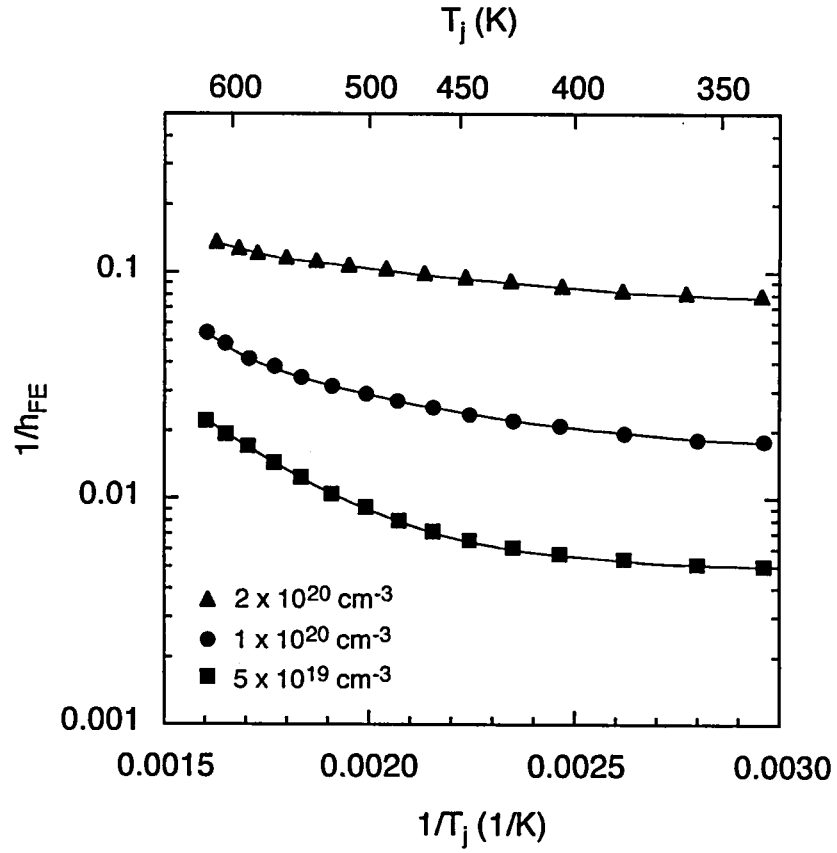


Fig. 3-7. Arrhenius plots of current gains of HBTs with base concentrations N_B of 5×10^{19} , 1×10^{20} , and $2 \times 10^{20} \text{ cm}^{-3}$. The data are taken at J_C of $1 \times 10^4 \text{ A/cm}^2$.

Auger recombination process, as mentioned previously. At higher T_j , the $1/h_{FE}$ varies exponentially with $1/T_j$. This signifies that the back injection of holes affects the current gain. Furthermore, the variation of the $1/h_{FE}$ with temperature decreases as N_B increases. This result indicates that the ΔE_{Veff} decreases by increasing N_B . The ΔE_{Veff} is evaluated by fitting the data to Eqs. (3-1), (3-3), and (3-9). The evaluated ΔE_{Veff} 's for N_B of 5×10^{19} , 1×10^{20} , and $2 \times 10^{20} \text{ cm}^{-3}$ are 0.33, 0.27, and 0.16 eV, respectively.

The ΔE_{Veff} 's at N_B higher than $3 \times 10^{20} \text{ cm}^{-3}$ could not be evaluated accurately because the variation of the $1/h_{FE}$ with temperature was relatively small. Therefore, the ΔE_{Veff} 's at higher doping levels were estimated by using the calculated ΔE_F , and the evaluated ΔE_V and ΔE_{BGN} . Both ΔE_V and ΔE_{BGN} were investigated by evaluating ΔE_C and ΔE_G . The ΔE_C , evaluated from the difference between turn-on voltage corresponding to J_C in a forward Gummel plot and J_E in a reverse Gummel plot [24], was about 0.08 V. The bandgaps of InGaP and GaAs were measured by the photoluminescence method to determine ΔE_G and ΔE_{BGN} . The bandgap of the InGaP emitter was 1.89 eV. On the other hand, the bandgap of the p -GaAs base varies with the base doping concentration, as shown in Fig. 3-8. The data show a variation as $N_B^{1/3}$ and is represented by

$$E_g (\text{eV}) = 1.43 - 1.2 \times 10^{-8} N_B^{1/3}, \quad (3-10)$$

which is similar to the bandgap obtained by Casey and Stern [25]. Based on these results and the calculated ΔE_F , the ΔE_{Veff} was estimated on the assumption that the ΔE_{BGN} simply increases ΔE_G ; i.e., $\Delta E_V = \Delta E_G + \Delta E_{BGN} - \Delta E_C$. The result is shown as the dashed line in Fig. 3-9. The ΔE_{Veff} becomes smaller than the ΔE_V at N_B of over $3 \times 10^{19} \text{ cm}^{-3}$, indicating that the large increase in the ΔE_F strikingly reduces the effective barrier height of holes. The evaluated ΔE_{Veff} 's from measured temperature dependence of current gain are also shown as solid circles. The estimated ΔE_{Veff} is slightly larger than the measured ΔE_{Veff} . The difference is probably because the effects of the ΔE_F and the ΔE_{BGN} were separately considered. However, their dependence on the carrier concentration is almost the same, and the measured results can be fitted when ΔE_{BGN} is assumed to be $0.6 \times 10^{-8} N_B^{1/3} \text{ eV}$, instead of $1.2 \times 10^{-8} N_B^{1/3} \text{ eV}$. The fitted ΔE_{Veff} is also shown as the solid line in Fig. 3-9.

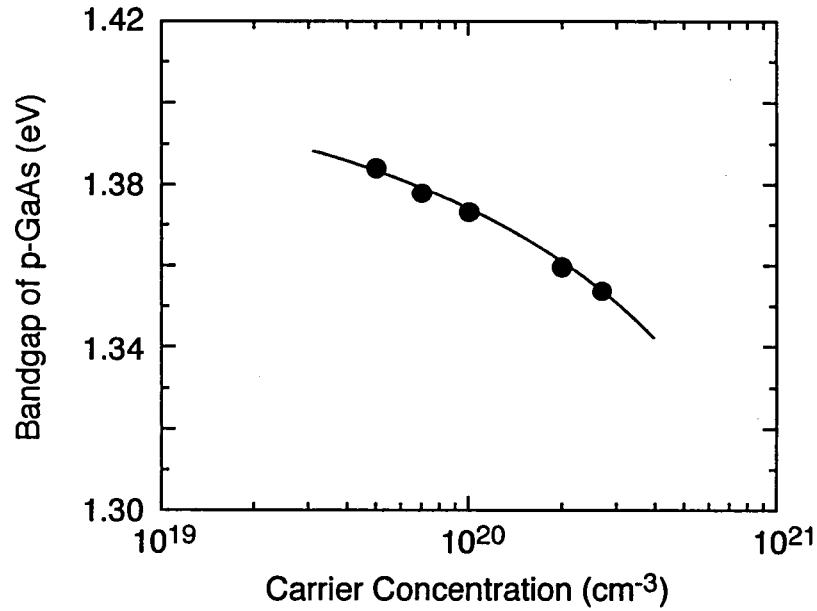


Fig. 3-8. Bandgap of *p*-GaAs estimated by the photoluminescence at room temperature as a function of carrier concentration.

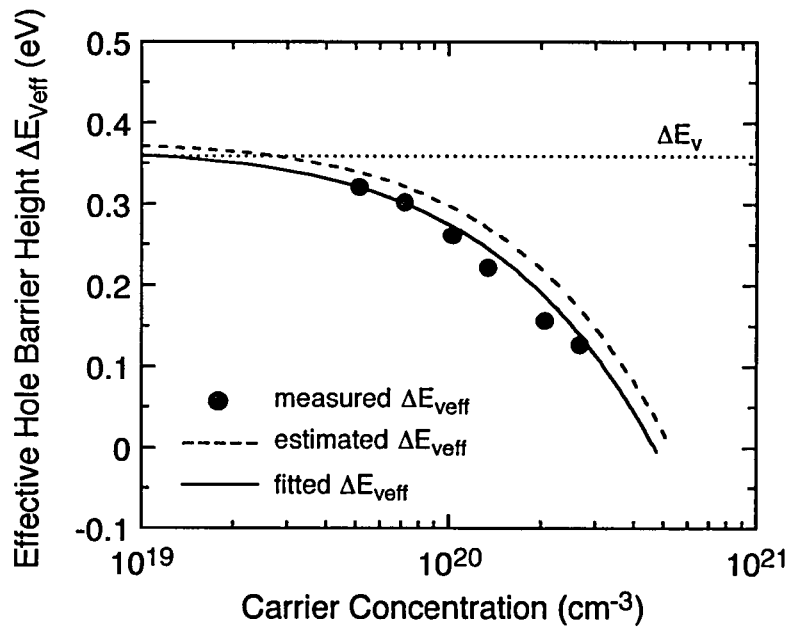


Fig. 3-9. Measured and estimated effective barrier heights of holes $\Delta E_{v\text{eff}}$. Also shown is $\Delta E_{v\text{eff}}$ fitted to the measured result. The dotted line indicates the valence band discontinuity ΔE_v .

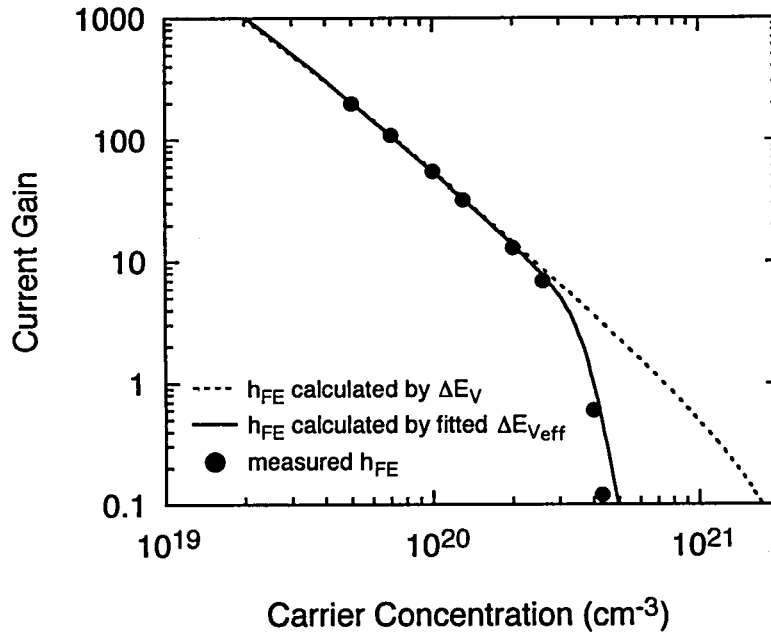


Fig. 3-10. Dependence of current gain h_{FE} on base concentration N_B calculated by using ΔE_V and fitted ΔE_{Veff} . Also shown are the measured results.

Finally, the current gain was examined by using the $\Delta E_{\nu eff}$ fitted to the measured results. Figure 3-10 shows the current gains calculated by using ΔE_{ν} and the fitted $\Delta E_{\nu eff}$. At N_B above $3 \times 10^{20} \text{ cm}^{-3}$, the measured current gains, shown as solid circles in Fig. 3-10, are almost consistent with the current gains calculated by using the fitted $\Delta E_{\nu eff}$. This indicates that the drastic reduction of the current gain at N_B above $3 \times 10^{20} \text{ cm}^{-3}$ can be explained by the increase in the back injection of holes caused by the reduction of the effective hole barrier height. The measured current gains are slightly below the solid curve. This result can be attributed to the increase in the recombination due to the reduction of the lifetime in the neutral base region [15]. The current gains calculated by using the fitted $\Delta E_{\nu eff}$ become less than unity at N_B of around $4 \times 10^{20} \text{ cm}^{-3}$. This result indicates that the highest base doping level for obtaining current gains more than unity is limited up to $4 \times 10^{20} \text{ cm}^{-3}$ for the GSMBE system utilized in this study even though the crystalline quality is improved. Although the limit of the doping level can be varied with different epitaxial systems due to the different ΔE_C , and thus ΔE_{ν} [26-32], suitable base doping concentration to obtain an appropriate current gain in InGaP/GaAs HBTs is surmised to be less than $1 - 2 \times 10^{20} \text{ cm}^{-3}$.

3.4 Effects of Base Thickness

3.4.1 Experimental results and discussions

The influences of the base thickness W_B on DC and high-frequency characteristics were investigated by current gains and delay time analysis.

Figure 3-11 shows the dependence of the current gain h_{FE} on the base thickness W_B evaluated from Gummel plots at a collector current density J_C of $1 \times 10^4 \text{ A/cm}^2$. The dependence varies at W_B around 30 nm: the h_{FE} is inversely proportional to the square of W_B at W_B larger than 30 nm; while the h_{FE} is inversely proportional to W_B at smaller W_B .

As discussed in the previous section, h_{FE} at N_B of $1 \times 10^{20} \text{ cm}^{-3}$ is determined by the recombination in the bulk base region, which is generally expressed as [33-35]

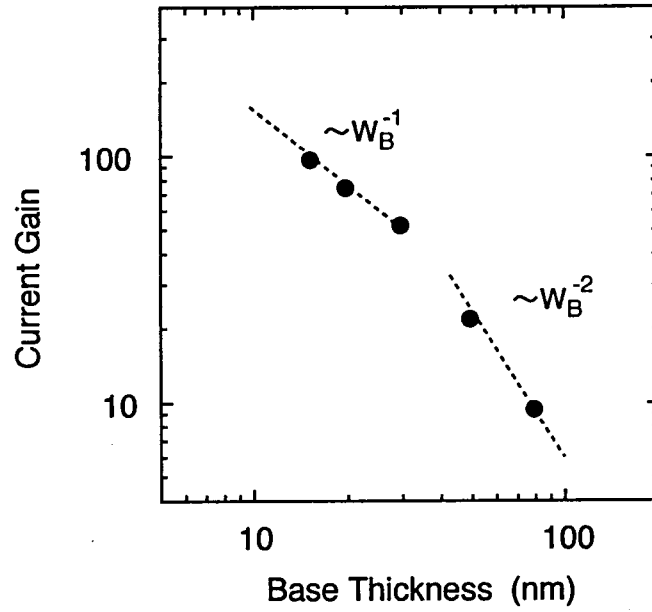


Fig. 3-11. Dependence of current gain h_{FE} on base thickness W_B .

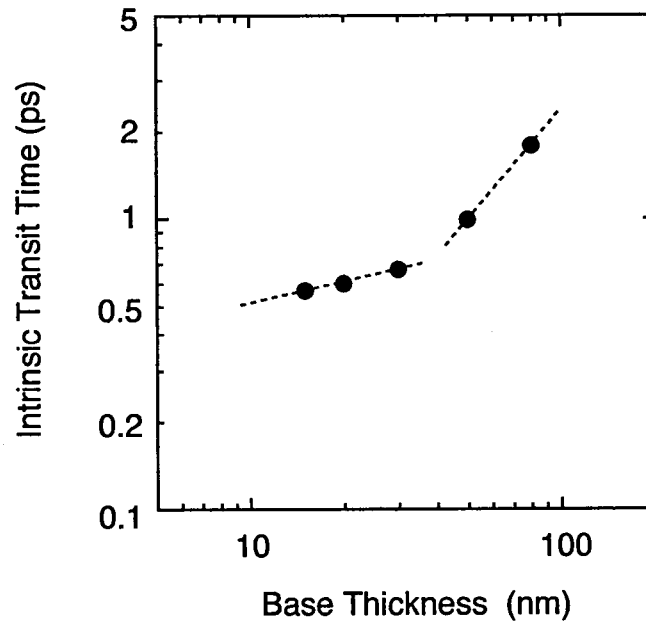


Fig. 3-12. Dependence of intrinsic transit time τ_F on base thickness W_B .

$$h_{FE} = \frac{\tau_n}{\tau_B}, \quad (3-11)$$

where τ_n is the minority carrier lifetime in the neutral base region and τ_B is the base transit time. When electron transport is diffusive, τ_B is given by [17]

$$\tau_B = \frac{W_B^2}{2D_n}, \quad (3-12)$$

where D_n is the diffusion coefficient of electrons in the base. In a very thin base, in contrast, insufficient scattering of electrons makes the transport nonequilibrium [36,37], and τ_B is expressed as [8]

$$\tau_B = \frac{W_B}{v_B}, \quad (3-13)$$

where v_B is the mean velocity of electrons in the base. Therefore, the dependence in Fig. 3-11 implies the relation between W_B and τ_B : the τ_B shows quadratic dependence on W_B at W_B larger than 30 nm, indicating that the electron transport in the base obeys the conventional diffusion model; whereas the τ_B tends to show linear dependence at smaller W_B , suggesting that nonequilibrium electron transport occurs.

Figure 3-12 shows the dependence of the intrinsic transit time τ_F , the sum of τ_B and the collector transit time τ_C , on W_B . The τ_F was estimated from the dependence of cutoff frequency on collector currents and the measured device parameters by using the method described in chapter 2. The dependence of τ_F also varies at W_B around 30 nm, which is the same as the result of the current gain, as shown in Fig. 3-11. This result suggests that the variation of τ_F is mainly influenced by the variation of τ_B ; i.e., the τ_C is not changed significantly at W_B ranging from 15 to 80 nm.

3.4.2 Effects on high-frequency performance

Based on the above results, τ_B and τ_C were analyzed as follows. When W_B is larger than 30 nm, the electron transport is diffusive. Therefore, τ_B and τ_C at W_B over 30 nm can be

deduced from the τ_F dependence on W_B by expressing $\tau_F = aW_B^2 + \tau_C$, where a is a constant, and τ_C is independent of W_B [38]. In contrast, τ_B at W_B less than 30 nm is estimated based on this result at W_B of 30 nm according as τ_B is inversely proportional to W_B , and τ_C is calculated by using the τ_B and τ_F .

Figure 3-13 shows the dependence of the deduced τ_B and τ_C on W_B . The τ_C does not change even at W_B of less than 30 nm, verifying that the variation of the intrinsic transit time mainly originates from the variation of τ_B , namely, the τ_C is almost constant at W_B ranging from 15 to 80 nm. The constant τ_C independent of W_B is probably ascribed to the relatively small ΔE_C (0.08 eV) [38]. The average electron velocity in the collector estimated from τ_C using Eq. (2-19) in chapter 2 is about 2.1×10^7 cm/s, which is in good agreement with that simulated on almost the same bias condition [39]. The dependence of the deduced τ_B on W_B is shown in Fig. 3-14.

As shown in Figs. 3-13 and 3-14, τ_B , and thus τ_F , can be effectively reduced by reducing W_B , especially when W_B is larger than 30 nm. However, τ_B is not effectively reduced because τ_B is in proportion to W_B , not W_B^2 , and as a result, τ_B occupies less than 1/3 in τ_F at W_B of less than 30 nm. This implies that the reduction of W_B is less effective for improving a cutoff frequency f_T . In contrast, the reduction of W_B monotonously increases the base sheet resistance and, thus, decreases a maximum oscillation frequency f_{\max} . Figure 3-15 shows an instance of the high-frequency characteristics of HBTs with W_B of 15 nm. While the extremely high f_T of 150 GHz is achieved, the f_{\max} is adversely as high as 70 GHz resulting from the large base resistance due to the thin base. This result signifies that W_B of less than 30 nm is not appropriate for achieving both high f_T and f_{\max} . Although the base resistance can be reduced by increasing the base doping concentration, the doping level higher than $1 - 2 \times 10^{20}$ cm⁻³ is not preferable for obtaining a moderate current gain, as discussed in the previous section. Hence, the optimum base thickness for achieving both high f_T and f_{\max} is summarized to be around 30 nm.

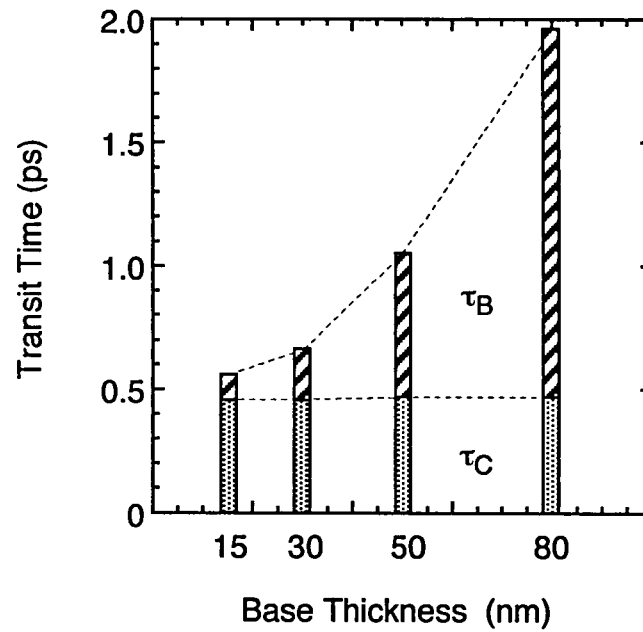


Fig. 3-13. Dependence of deduced base transit time τ_B and collector transit time τ_C on base thickness W_B .

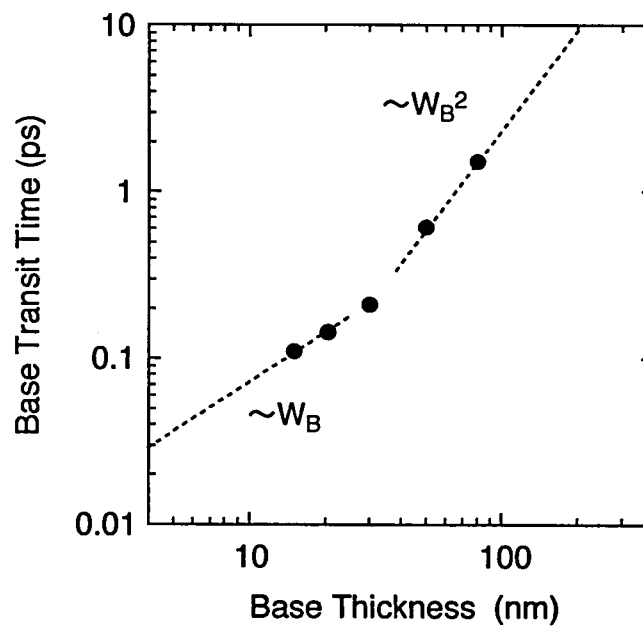


Fig. 3-14. Dependence of base transit time τ_B on base thickness W_B .

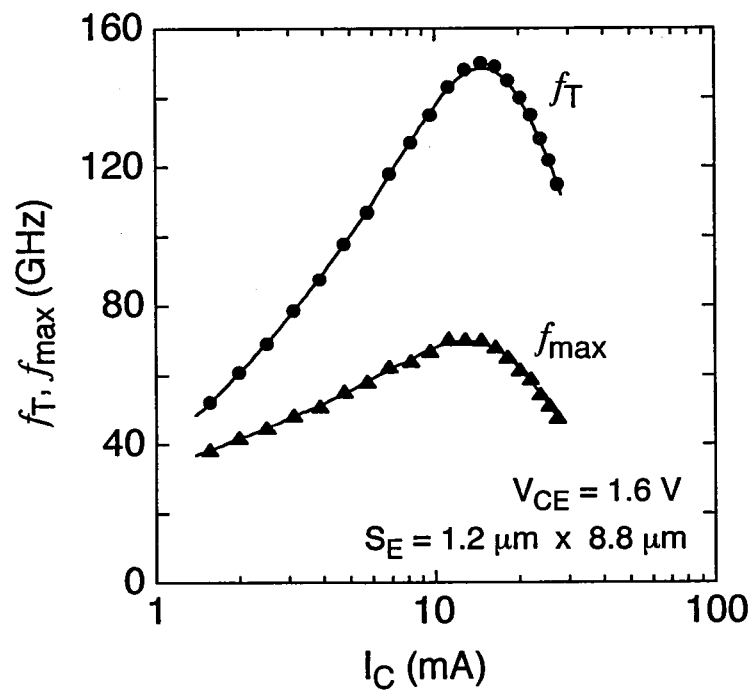


Fig. 3-15. f_T and f_{max} as a function of collector currents for fabricated HBT with W_B of 15 nm. The emitter size S_E is $1.2 \mu\text{m} \times 8.8 \mu\text{m}$ and the bias voltage V_{CE} is 1.6 V.

3.5 Summary

The effects of the base doping concentration N_B and the base thickness W_B on the characteristics of InGaP/GaAs HBTs were studied in detail in order to optimize the base layer design for high-speed operations. The current gain h_{FE} at N_B of less than $3 \times 10^{20} \text{ cm}^{-3}$ was inversely proportional to the square of N_B , indicating that the h_{FE} was determined by Auger recombination in the intrinsic base region. The h_{FE} at N_B above $3 \times 10^{20} \text{ cm}^{-3}$, in contrast, decreased drastically because of the increase in the back injection of holes. The dependence of h_{FE} on temperature showed that the barrier height of holes decreased as N_B increased. The reduction of the barrier height, i.e., the effective barrier height was explained analytically and experimentally by considering the bandgap narrowing and the Fermi level in accordance with the Fermi-Dirac distribution. Consequently, the optimum base doping concentration to obtain an appropriate current gain in InGaP/GaAs HBTs was estimated to be $1 - 2 \times 10^{20} \text{ cm}^{-3}$.

The base transit time τ_B was deduced from the dependences of the current gain and the intrinsic transit time τ_F on W_B . At W_B larger than 30 nm, the τ_B exhibited a quadratic dependence on W_B , whereas the τ_B tended to show a linear dependence at smaller W_B . The collector transit time τ_C , on the other hand, was estimated to be independent of W_B . As a result, the τ_B , and thus τ_F , can be effectively reduced by reducing W_B at W_B of larger than 30 nm; whereas τ_B is not effectively reduced at W_B of less than 30 nm, which made τ_B occupy less than 1/3 in τ_F . In considering the increase in the base resistance and the base doping level for obtaining a moderate current gain, the optimum base thickness for achieving both high f_T and f_{\max} was inferred to be around 30 nm.

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Chapter 4

InGaP/GaAs HBTs with WSi/Ti Base Electrode and Buried SiO₂ in the Extrinsic Collector

4.1 Introduction

As stated in chapter 1, GaAs-based HBTs are more attractive for high-speed applications than Si bipolar devices due to their superior carrier transport properties [1,2]. Thus, they have been widely developed for applying to high-speed integrated circuits such as optical-fiber communication systems and microwave or millimeter-wave wireless communication systems [3-7]. To date, GaAs HBTs with high cutoff frequency f_T over 100 GHz [8] and high maximum oscillation frequency f_{max} over 200 GHz [9,10] have been exhibited. However, these HBTs have considerably large device dimensions compared to Si BJTs and SiGe HBTs. Therefore, GaAs HBTs require large collector currents in order to operate at high frequency. This causes large power dissipation as well as thermal-management problems when they are applied to integrated circuits (ICs); especially highly integrated chips such as those used in high-speed communications.

To solve the problem of the large power dissipation, reduction of the emitter size is inevitable. For this reason, GaAs HBTs with small emitter sizes of equal to or smaller than 1 μm^2 have already been demonstrated [11-13]. However, their high-frequency characteristics

were drastically degraded as scaling down the device size. This is mainly due to the relatively large base-collector capacitance resulting from the large base-collector junction area, which increases the parasitic delay time of transistors. To reduce the base-collector capacitance, the self-aligned technique that the base-collector mesa is etched by using the base electrode as a wet-etching mask has been developed [14-16]. In this method, the base-collector junction area underneath the periphery of the base electrode is removed by the side etching, as shown in Fig. 3-1 in chapter 3. However, the extrinsic collector region used to contact the wire and the base electrode, which is not scaled down in proportion to the emitter size, still remains, as mentioned in chapter 2. Hence, the key to improve the high-frequency performance in small-scale GaAs HBTs is the reduction of the parasitic capacitance originating from the extrinsic collector under the base contact pad region.

One extensively utilized approach to reducing such parasitic capacitance is to perform proton or oxygen ion implantation into the extrinsic collector regions [17,18]. The implanted ions compensate the relatively low doping of the collector, thus fully depleting the extrinsic collector regions. While this approach has improved high-frequency performance, the extrinsic collector region remains as an integral part of the overall transistor mesa, whose dielectric constant is still as large as that of GaAs, and thus still contributes to a certain amount of parasitic capacitance. Furthermore, ion implantation increases the base resistance, which also degrades the high-frequency characteristics. To eliminate the parasitic capacitance completely, deletion of the subcollector layer under the base contact pad region has been studied by using deep ion implantation or regrowth technique [19-22]. However, these techniques require a high-energy ion-implantation apparatus or a complex regrowth process, and they also can have problems due to the ion-implantation damage or the poor quality of the regrowth interface.

In this chapter, the author proposes a novel device structure with process technology aimed at physically removing the GaAs in the extrinsic collector underneath the base contact pad region. The process technology utilizes a buried SiO₂ in the extrinsic collector region. The technology also utilizes WSi/Ti as the base electrode, which simplifies and facilitates the processing to fabricate such an HBT structure with buried SiO₂. The proposed device structure realizes the reduction of parasitic capacitance with the simultaneous scaling down

of the emitter size and, consequently, enables the excellent high-frequency operation at a low collector current.

4.2 Proposal of Novel Device Structure

Schematic cross section and layout of the proposed device structure are illustrated in Fig. 4-1. The structure has the following two main features.

One feature is that the width of the base contact is reduced to $0.3\ \mu\text{m}$ by using a self-aligning process, and the extrinsic collector region under the base electrode is buried by SiO_2 . The buried SiO_2 reduces the parasitic capacitance in the extrinsic collector because the dielectric constant of SiO_2 is about $1/3$ of that of GaAs [23]. Narrowing the width of the base contact also reduces the base-collector capacitance because it decreases the base-collector junction area.

Another feature is that WSi/Ti metals are used as the base electrode. WSi has definite advantages over conventional gold-based electrode metals; i.e., it can be deposited by a sputtering method with good step coverage and selectively patterned on GaAs and SiO_2 by using reactive ion etching (RIE). These advantageous properties simplify the processing and enable the fabrication of base electrodes of small-scale HBTs with narrow base contacts and buried SiO_2 [24]. In addition, a thin Ti film inserted between WSi and p -type GaAs effectively reduces the contact resistance compared to using WSi only, as discussed in the next section. This suppresses the large increase in the base resistance that occurs when reducing the width of the base contact, and therefore, makes it possible to achieve much higher frequency performance.

All these features simultaneously enable both the scaling down of the emitter size and the reduction in the parasitic capacitance of the base-collector junction, leading to high-speed operation of GaAs HBTs at low collector currents.

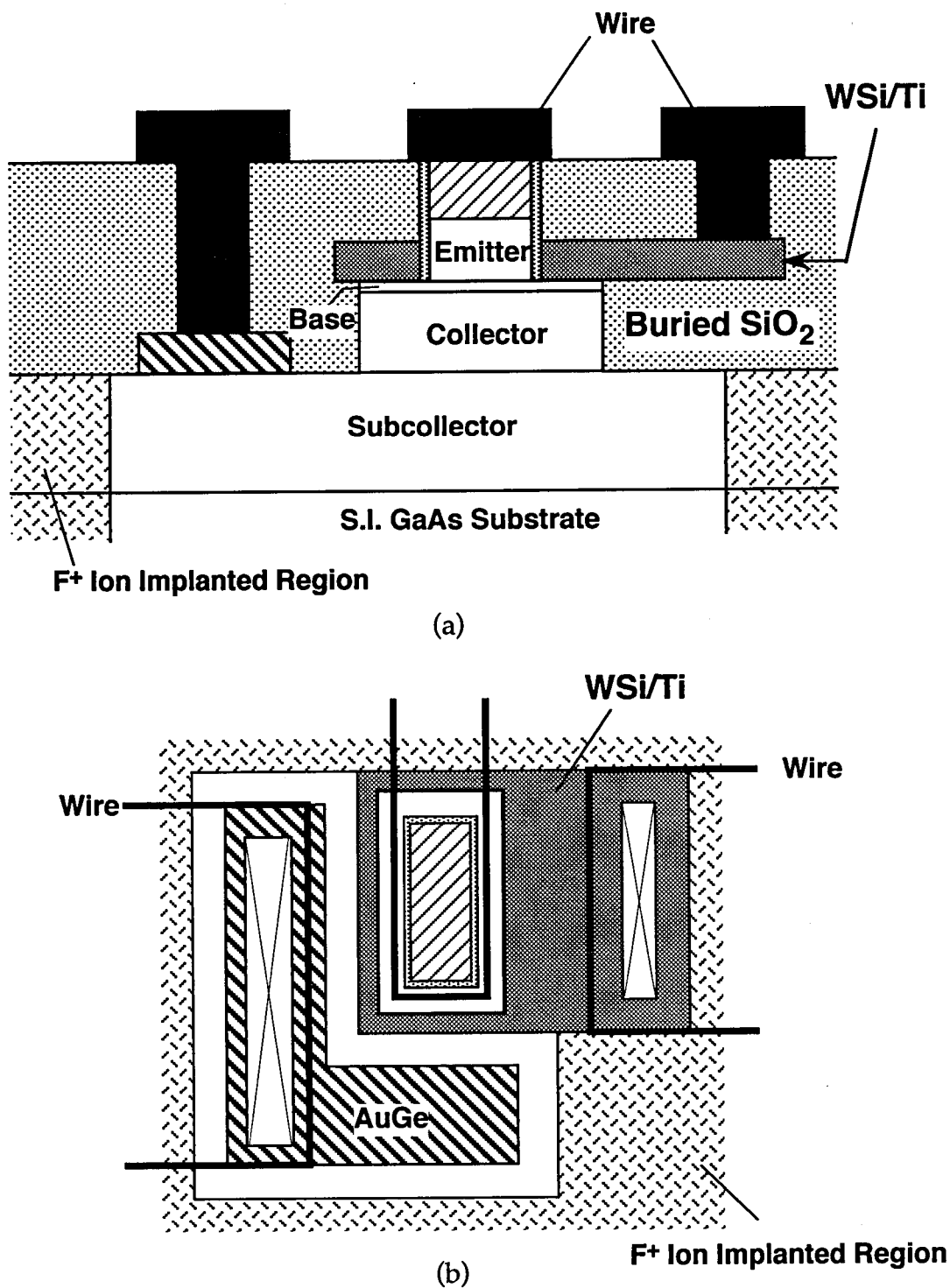


Fig. 4-1. (a) Schematic cross-section and (b) layout of proposed HBT structure with WSi/Ti base electrode and buried SiO_2 .

4.3 Characteristics of WSi/Ti Ohmic Contact

Before discussing the device fabrication, the ohmic contact characteristics of WSi/Ti metals for p -GaAs are investigated. In order to design HBTs with both high f_T and high f_{\max} , the optimum width of the base contact is also estimated.

4.3.1 Contact Resistance of WSi for p -GaAs

Firstly, the possibility of WSi as the ohmic metal for p -GaAs was investigated. The specific contact resistance ρ_c between p -GaAs and WSi was evaluated by a transmission line model (TLM) measurement [25,26]. Actual HBT wafers, as explained in the next section, were prepared for these experiments. The base layer was 30-nm thick and the hole concentration N_B varied from 5×10^{19} to $4 \times 10^{20} \text{ cm}^{-3}$, where the sheet resistances were in the range of 620 to 160 Ω/square . The layout of the TLM patterns and the cross-sectional view of the pattern are shown in Fig. 4-2. The line width W of the TLM patterns was 10 μm , and the spacing L between the pads was 2, 4, 8, 16 and 32 μm . The 300-nm thick WSi_x films were deposited on the base layers through patterned SiO_2 holes by a sputtering method. The composition ratio x was 0.3, and the sheet resistance of the 300-nm-thick WSi was approximately 7 Ω/square . A native oxide on p -GaAs was removed by dilute HF solution before WSi deposition. Au/Pt/Ti metals were deposited on WSi as the contact pad for probing.

The specific contact resistance ρ_c as a function of carrier concentration N_B is shown in Fig. 4-3. The dashed lines are calculated theoretical curves of the relationship between ρ_c and N_B , corresponding to various potential barrier heights ϕ_B . The calculation was carried out based on the field-emission theory, known as a tunneling model, expressed as [27]

$$\rho_c = \left[\frac{A\pi q}{kT \sin(\pi c_1 kT)} \exp\left(\frac{-\phi_B}{E_{00}}\right) - \frac{Ac_1 q}{(c_1 kT)^2} \exp\left(\frac{-\phi_B}{E_{00}} - c_1 u_F\right) \right]^{-1}, \quad (4-1)$$

where

$$c_1 = \frac{1}{2E_{00}} \ln\left(\frac{4\phi_B}{u_F}\right), \quad (4-2)$$

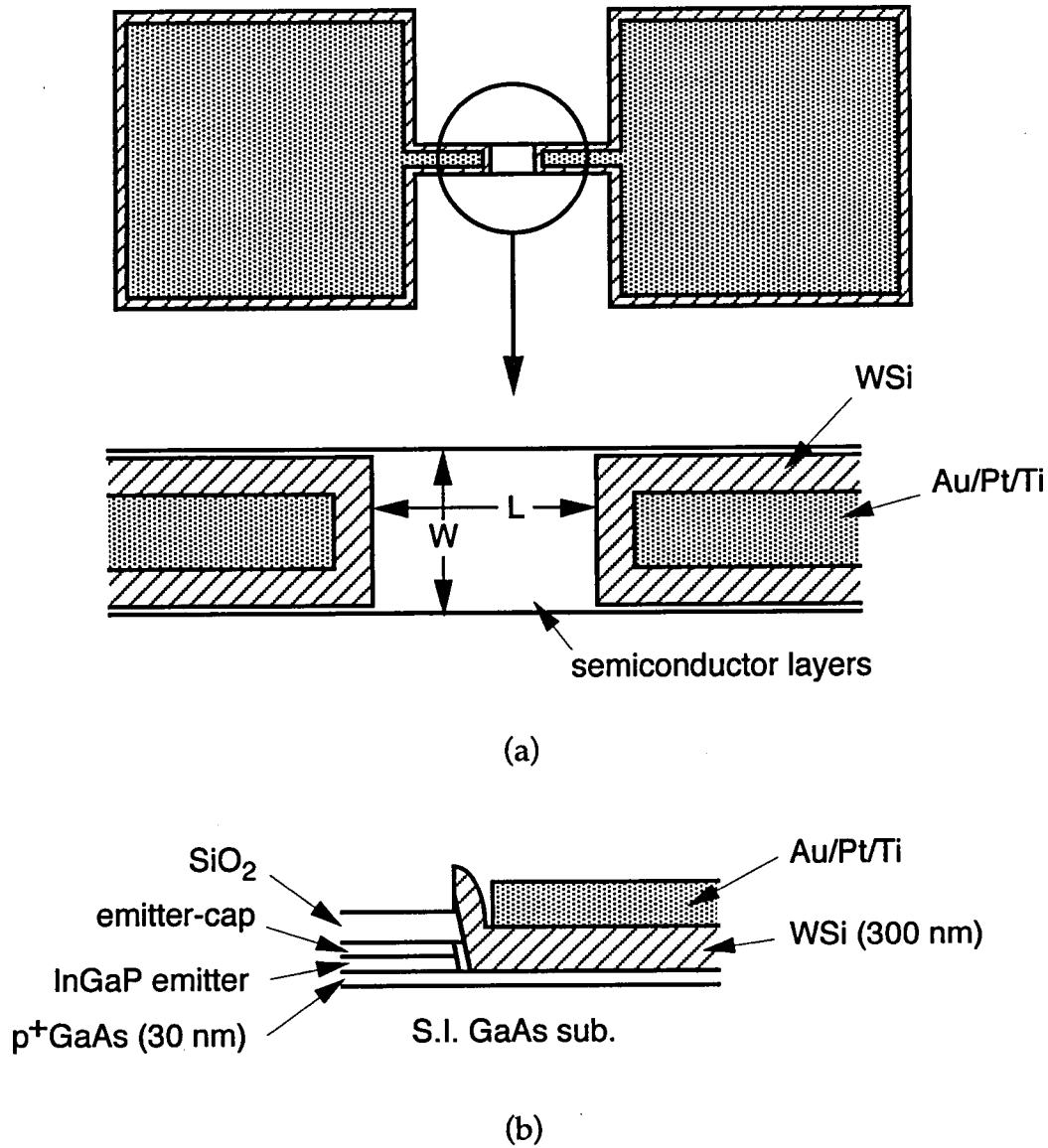


Fig. 4-2. Layout of TLM patterns and its cross sectional view: (a) layout patterns; (b) cross section.

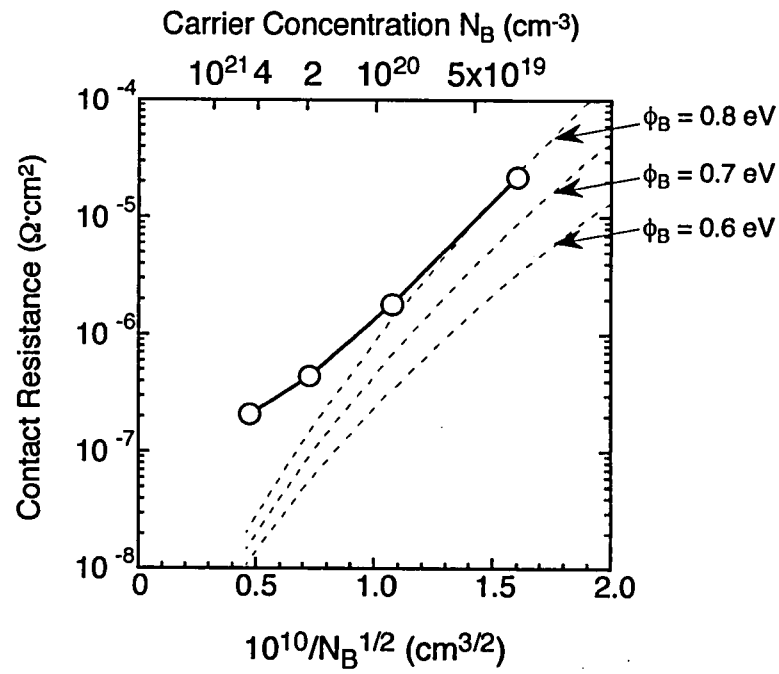


Fig. 4-3. Specific contact resistance for WSi as a function of carrier concentration N_B in 30-nm-thick p -type GaAs.

$$A = \frac{4\pi m^* q (kT)^2}{h^3} \quad (4-3)$$

is the Richardson constant times T^2 , m^* the effective mass of holes, ϕ_B the Schottky barrier height, and u_F the Fermi level measured from the valence band maximum. E_{00} is the characteristic energy given by

$$E_{00} = \frac{qh}{4\pi} \sqrt{\frac{N_B}{m^* \epsilon}}, \quad (4-4)$$

where ϵ is the dielectric constant of GaAs. In this calculation, $\epsilon/\epsilon_0 = 13.1$ and $m^*/m_0 = m_{lh}^*/m_0 = 0.082$ are used [23], where ϵ_0 is the permittivity in vacuum and m_0 is the mass of free electron. As shown in Fig. 4-3, the ρ_c fits the theoretical curve for ϕ_B of 0.8 eV at the lower carrier concentration, indicating that WSi can be used as a non-alloyed ohmic electrode for heavily-doped p -GaAs at N_B higher than $5 \times 10^{19} \text{ cm}^{-3}$. However, the contact resistance is relatively large compared to conventionally utilized Au/Pt-based metals. At a carrier concentration of $1 \times 10^{20} \text{ cm}^{-3}$, for example, ρ_c for WSi is $2 \times 10^{-6} \Omega \cdot \text{cm}^2$, which is about one order of magnitude higher than that for Au/Pt-based metal [28]. Although the lower ρ_c can be obtained at the higher N_B , the ρ_c deviates to higher ϕ_B as the carrier concentration increases. The suppression of the ρ_c reduction is probably ascribed to the interfacial oxide between WSi and GaAs [29]. Since the higher N_B also gives rise to the extreme reduction in current gain by increasing the back injection of holes into the emitter, as discussed in chapter 3, the decrease in ϕ_B is inevitable to improve the high-frequency performance of the proposed device structure.

4.3.2 Effect of Ti Insertion

As the ohmic contact metal for p -GaAs, various kinds of material systems with Pt or Ti as the ground layer, such as Pt/Ti, Au/Pt/Ti, and Au/Pt/Ti/Pt, were studied as a stable non-alloy ohmic electrode [29-32]. Pt-based ohmic systems, in particular, have been widely utilized because of its large work function, which is effective to reduce the hole barrier height.

However, Pt is not usable in the proposed device fabrication because Pt is not sufficiently adhesive to SiO₂. To reduce the contact resistance for WSi systems, therefore, insertion of a thin Ti layer between *p*-GaAs and WSi was examined.

Figure 4-4 shows the dependence of ρ_c at N_B of $1 \times 10^{20} \text{ cm}^{-3}$ on the thickness of inserted Ti layer. The contact resistance was reduced to $2 - 3 \times 10^{-7} \Omega \cdot \text{cm}^2$ when the Ti layer was thicker than 5 nm. This implies that Ti insertion as thin as 5 nm effectively reduces the contact resistance; that is, the contact resistance is determined by the less than 5-nm thick Ti layer close to the *p*-GaAs surface. The ρ_c of WSi and WSi/Ti (5 nm) as a function of carrier concentration N_B is shown in Fig. 4-5. All these ρ_c values of WSi/Ti are about one order of magnitude lower than those of WSi. The ρ_c of WSi/Ti agrees well with the curve for ϕ_B of 0.6 eV at any carrier concentration. These results indicate that the insertion of the thin Ti film effectively decreases the potential barrier height and thus reduces the contact resistance.

To investigate the effect of the Ti insertion, the interface was observed by a transmission electron microscope (TEM) equipped with an energy dispersive X-ray spectrometer (EDX), and in-depth profiles were measured by Auger electron spectroscopy (AES) with Ar⁺-ion sputtering. Figure 4-6 shows the TEM cross sections of the samples with an inserted Ti thickness of 5 nm and 20 nm. In both cross sections, an amorphous layer with a thickness of about 2 nm was observed. EDX revealed that the amorphous layer mainly consisted of Ti exists between GaAs and Ti crystal layers. Figure 4-7 shows the AES depth profiles of WSi/Ti on GaAs with a Ti thickness of 20 nm. Oxygen slightly exists in the vicinity of Ti/GaAs interface. These results suggest that the amorphous layer is formed by the reaction of Ti with a native oxide on the GaAs surface, and therefore, the lower contact resistance than that without Ti insertion is probably attributed to the formation of quasi-oxide-free interface between Ti and *p*-GaAs due to the high reactivity of Ti [33,34]. Since the native oxide on the GaAs surface is speculated to be as thick as 2 nm, Ti insertion as thin as 5 nm is enough for reducing the contact resistance of WSi systems.

4.3.3 Optimization of Base Contact Width

Narrowing the width of the base contact W_{BC} is indispensable to decrease the

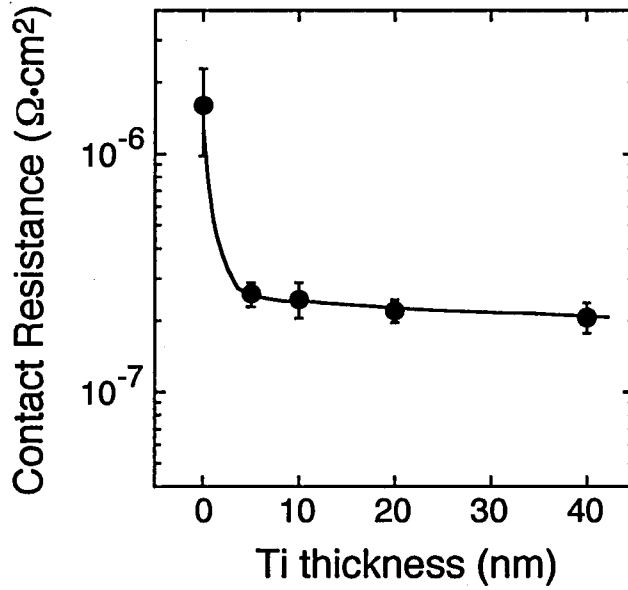


Fig. 4-4. Dependence of specific contact resistance at N_B of $1 \times 10^{20} \text{ cm}^{-3}$ on thickness of inserted Ti layer.

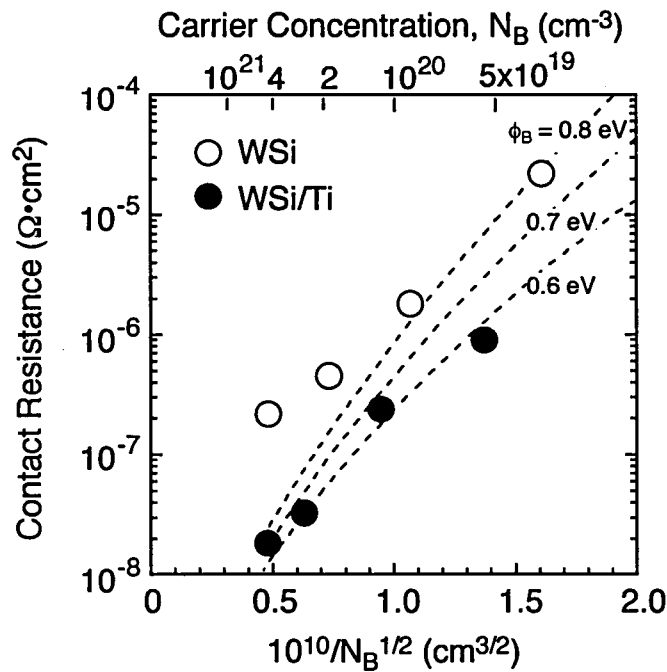


Fig. 4-5. Specific contact resistance for WSi and WSi/Ti as a function of carrier concentration N_B in p -GaAs layers.

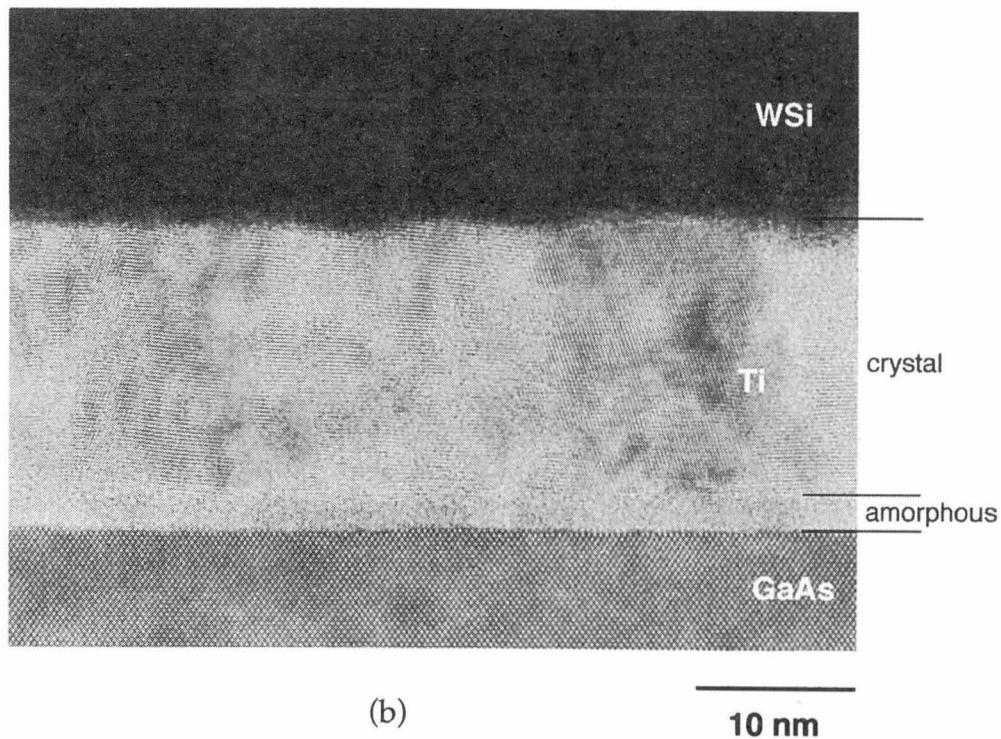
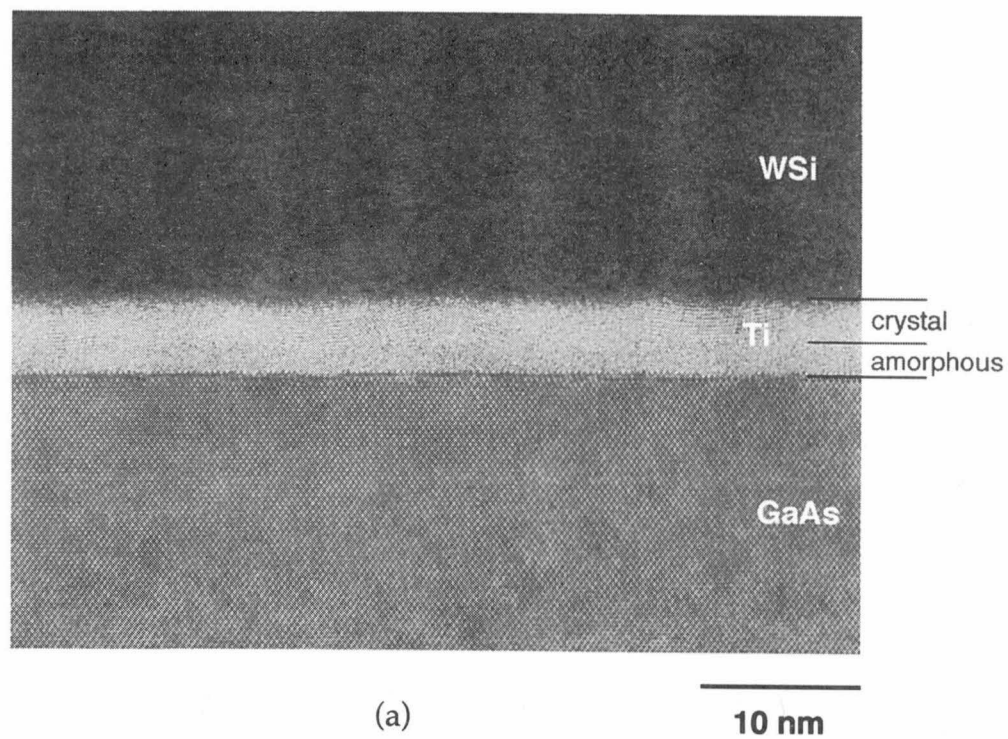


Fig. 4-6. TEM cross sections of the samples with inserted Ti thickness of (a) 5 nm and (b) 20 nm.

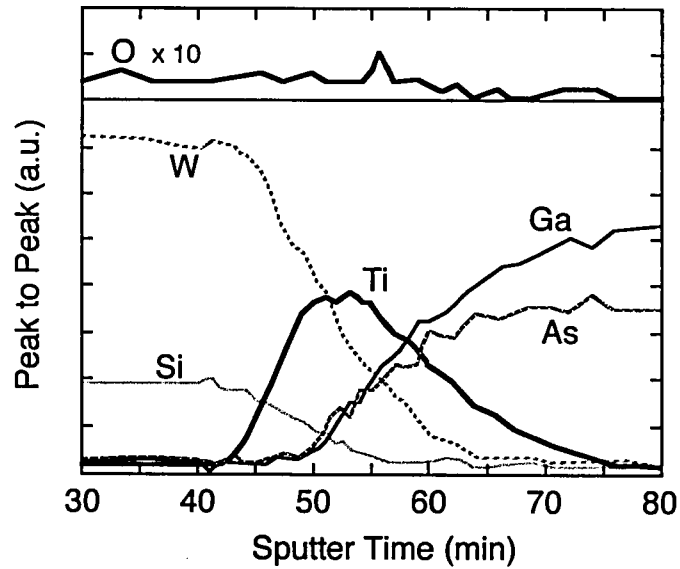


Fig. 4-7. AES depth profiles of WSi/Ti on GaAs with Ti thickness of 20 nm.

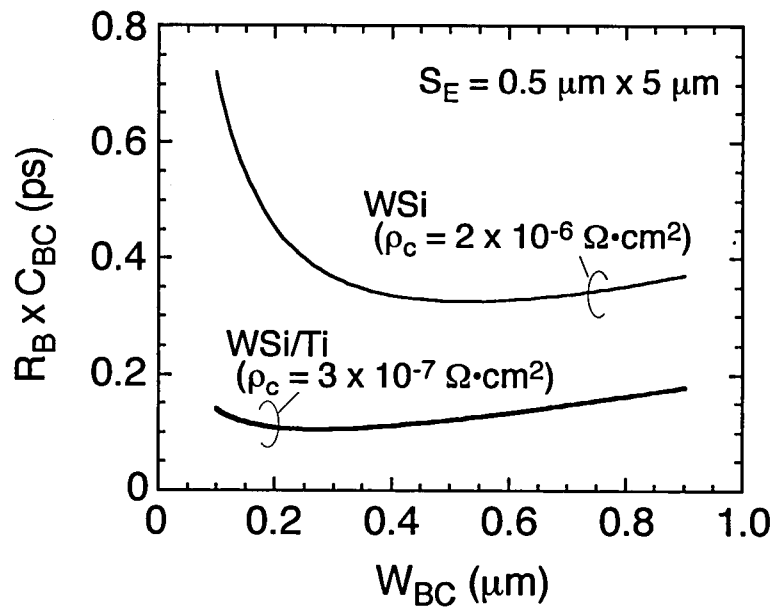


Fig. 4-8. Calculated product of base resistance R_B and base-collector capacitance C_{BC} as a function of base-contact width W_{BC} .

base-collector capacitance C_{BC} and thus increase both f_T and f_{max} . However, the narrow contact width simultaneously increases base resistance R_B , which degrades f_{max} . This means that W_{BC} has an optimum value for attaining both high f_T and high f_{max} . In order to optimize the device design around the base contact region, therefore, the dependence of the product of R_B and C_{BC} on W_{BC} was estimated.

Figure 4-8 shows the calculated product of R_B and C_{BC} of a device with an emitter size S_E of $0.5 \mu\text{m} \times 5 \mu\text{m}$ and a base doping concentration of $1 \times 10^{20} \text{ cm}^{-3}$. The calculation was carried out by assuming that the device structure was as described in the next section. The product for the case of the WSi base electrode reaches its minimum at W_{BC} of $0.55 \mu\text{m}$ and rapidly increases when W_{BC} is below $0.4 \mu\text{m}$. On the other hand, the product for the WSi/Ti electrode is about 1/2 to 1/3 smaller than that for the WSi electrode. The product shows the minimum at W_{BC} of $0.25 \mu\text{m}$ and it does not show the remarkable increase even though W_{BC} is less than $0.2 \mu\text{m}$. These results are due to the extremely low ρ_c of WSi/Ti, suggesting that W_{BC} can be reduced to less than $0.4 \mu\text{m}$ without greatly increasing base resistance. It should be noted that the optimum value of W_{BC} can be slightly changed according to the emitter size. However, the proposed HBT structure would reach both high f_T and f_{max} at W_{BC} of around 0.2 to $0.3 \mu\text{m}$.

4.4 Fabrication Process

The epitaxial layers were grown by GSMBE, the details of which were described in chapter 2. The parameters of the epitaxial layer structure are listed in Table 4-1. The emitter-cap layers consist of highly doped n -InGaAs (50 nm, $n = 4 \times 10^{19} \text{ cm}^{-3}$), n -GaAs (100 nm, $n = 8 \times 10^{18} \text{ cm}^{-3}$), and n -InGaP (50 nm, $n = 8 \times 10^{18} \text{ cm}^{-3}$) to reduce the emitter resistance. The emitter layer is 100-nm InGaP doped to $5 \times 10^{17} \text{ cm}^{-3}$. The p -GaAs base layer is highly doped to $1.3 \times 10^{20} \text{ cm}^{-3}$ to reduce the contact resistance with the WSi/Ti base electrode, and the thickness is 30 nm to obtain an appropriate current gain at the high base doping level. The n -GaAs collector layer is 200 nm thick and doped to $2 \times 10^{16} \text{ cm}^{-3}$. The n -GaAs subcollector layer is 800 nm thick and doped to $8 \times 10^{18} \text{ cm}^{-3}$. The relatively thick subcollector layer was used in order to bury the thick SiO_2 in the extrinsic collector, and the relatively high doping

Table 4-1. Parameters of epitaxial layer structure of fabricated HBTs.

Layer	Material	Doping Concentration (cm ⁻³)	Thickness (nm)
Emitter-cap	<i>n</i> -InGaAs	4 × 10 ¹⁹	50
	<i>n</i> -GaAs	8 × 10 ¹⁸	100
	<i>n</i> -InGaP	8 × 10 ¹⁸	50
Emitter	<i>n</i> -InGaP	5 × 10 ¹⁷	100
Base	<i>p</i> -GaAs	1.3 × 10 ²⁰	30
Collector	<i>n</i> -GaAs	2 × 10 ¹⁶	200
Subcollector	<i>n</i> -GaAs	8 × 10 ¹⁸	800

was due to the reduction of the collector resistance.

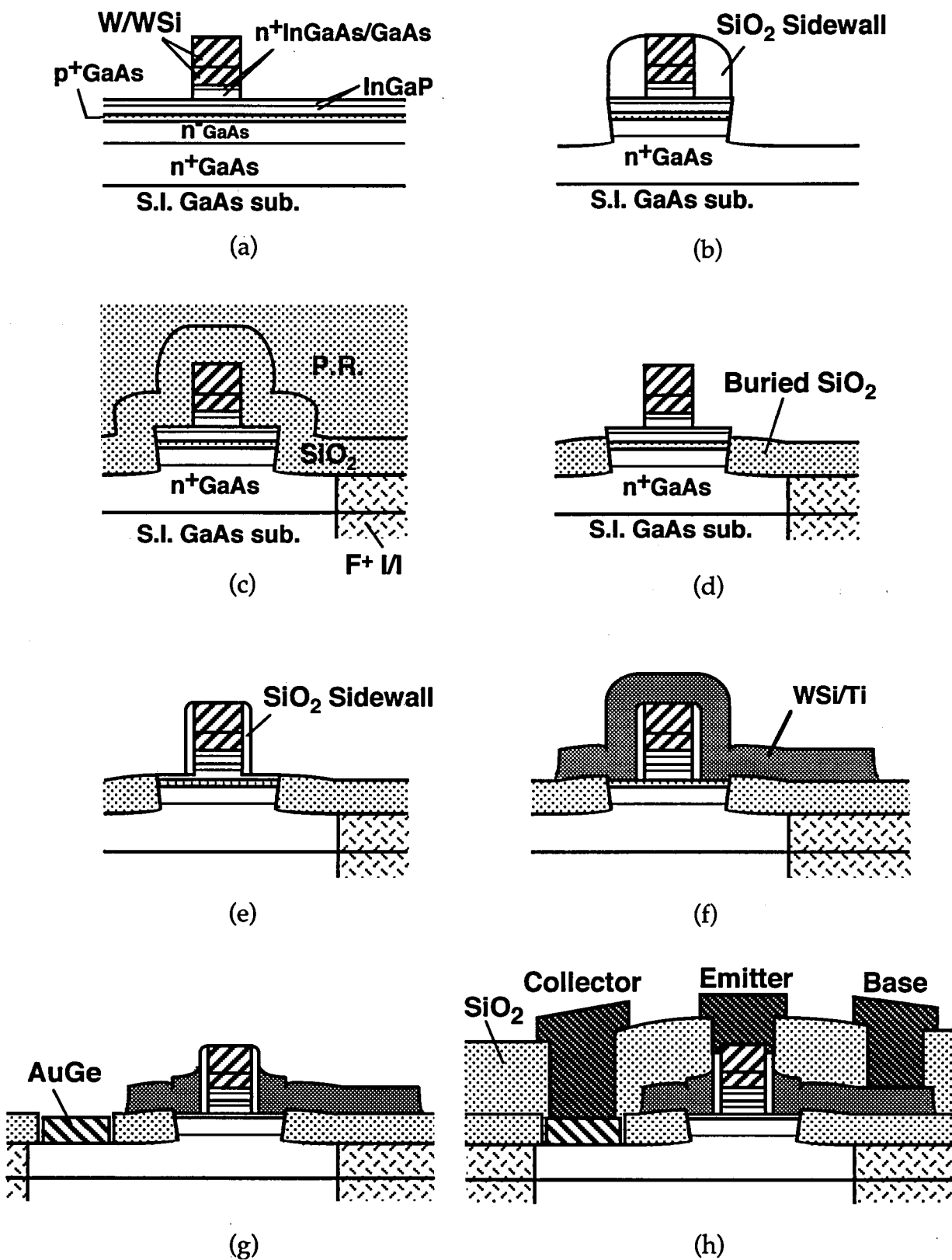
The main steps in the fabrication process are shown schematically in Fig. 4-9. The device fabrication starts with the deposition of W/WSi on the InGaAs emitter-cap layer by RF sputtering. These metals are formed into a non-alloyed emitter electrode by RIE using CHF_3 and SF_6 . By using the emitter electrode as an etching mask, the InGaAs and GaAs emitter-cap layers are etched by Cl_2/CH_4 electron cyclotron resonance (ECR) plasma [Fig. 4-9(a)].

This is followed by a thick SiO_2 sidewall formation around the emitter electrode and the emitter-cap mesas. By using this sidewall as an etching mask, the base-collector mesa is self-aligningly formed by ECR plasma etching [Fig. 4-9(b)].

After F^+ ions are implanted to isolate each device, thick SiO_2 for burying the outsides of the base and collector mesas is deposited and the wafer surface is planarized by photoresist [Fig. 4-9(c)]. The buried SiO_2 structure is then formed by a simultaneous etchback of both photoresist and SiO_2 [Fig. 4-9(d)].

Subsequently, the InGaP layers are etched by ECR plasma, remaining at least 50 nm unetched in order to avoid the plasma damage to the base surface. Then, a thin sidewall of SiO_2 is formed for separating the emitter and the base metal [Fig. 4-9(e)]. The thinner sidewall effectively decreases the device dimensions. However, the small emitter-base contact spacing induces the current gain reduction caused by the direct recombination at the base contact surface due to the lateral diffusion of electrons. When the base doping level is $1 \times 10^{20} \text{ cm}^{-3}$, more than 0.04 μm is necessary for avoiding the recombination at the base contact surface [35]. Therefore, the thickness of the sidewall was designed as 0.1 μm . According to the result discussed in the previous section, the optimum width of the base contact is around 0.2 to 0.3 μm . Consequently, the thickness of the sidewall for the base-collector mesa-etching shown in Fig. 4-9(b) was designed as 0.4 μm .

The remaining InGaP layer is removed by selective wet-chemical etching using a solution of dilute HCl to expose the base surface undamagedly. During this etching, the side of the emitter layer is almost unetched due to the dependence of the etching rate on the plane orientation of crystals. Subsequently, Ti and WSi metals are deposited by RF sputtering and etched by RIE and dilute HF to define the base electrode area, using photoresist as a mask

Fig. 4-9. Fabrication steps for proposed HBT with WSi/Ti base electrode and buried SiO₂.

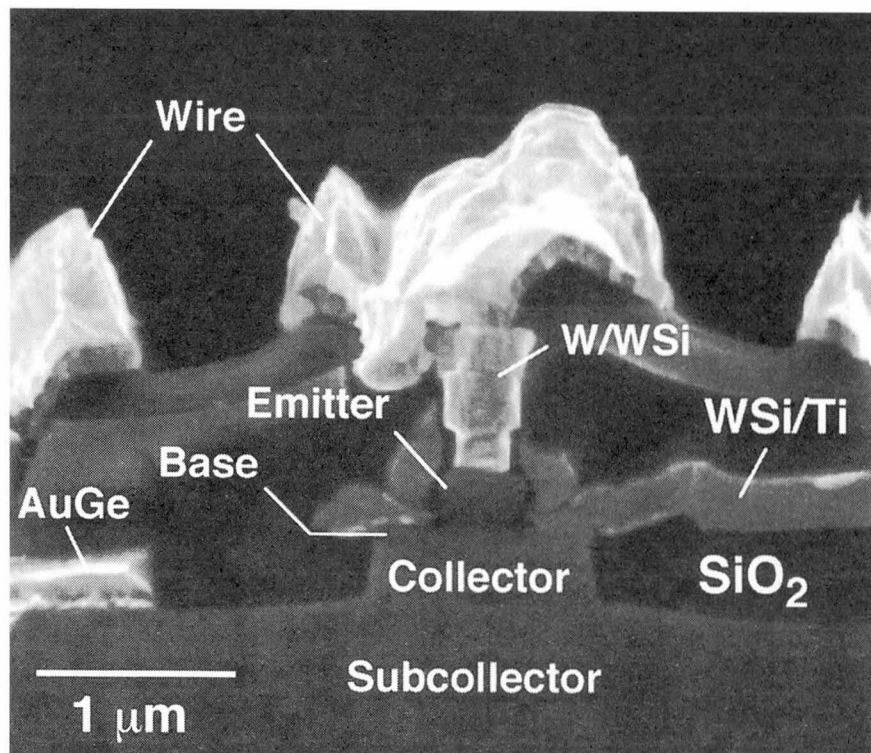


Fig. 4-10. SEM cross-section of the fabricated HBT with a WSi/Ti base electrode and buried SiO_2 .

[Fig. 4-9(f)].

AuGe/W/Ni/Au/Mo is then evaporated on the subcollector and formed as a collector electrode by a lift-off process, followed by alloying at 350°C for 30 minutes. Subsequently, the WSi on the emitter electrode is selectively etched by RIE with CF₄ by using a photoresist mask, and the Ti on the emitter electrode is removed by dilute HF [Fig. 4-9(g)]. Finally, the metallization process follows and the device structure is completed [Fig. 4-9(h)].

Figure 4-10 shows a cross-sectional scanning electron micrograph (SEM) of the developed HBT. The base contact width is about 0.3 μm and the sidewall thickness is almost 0.1 μm. The final thickness of the buried SiO₂ is about 0.4 μm. It is seen that the WSi/Ti base electrode covers both the narrow base contact surface and the buried SiO₂ outside of the base-collector junction, indicating that WSi and Ti are useful metals in fabricating the base electrodes for small-scale HBTs with a narrow contact region and buried SiO₂.

4.5 Device Performance

4.5.1 DC characteristics

The DC characteristics of the developed HBTs with various emitter sizes were evaluated by using an HP4145B semiconductor parameter analyzer.

The common-emitter $I_C - V_{CE}$ characteristics for the developed HBT with an emitter size S_E of 0.3 μm × 1.6 μm are shown in Fig. 4-11. The small signal current gain h_{fe} is 15, and a collector-emitter breakdown voltage BV_{CEO} of 10 – 11 V is attained. The offset voltage is about 0.25 V. This relatively large offset voltage is probably attributed to the relatively large ratio of the base-collector junction area to the emitter area as well as the difference in turn-on voltages of the base-emitter and the base-collector junction [36]. Figure 4-12 shows a Gummel plot for the HBT with an S_E of 0.3 μm × 1.6 μm. The ideality factors of the collector and the base currents are 1.0 and 1.6, respectively. The DC current gain h_{FE} of 20 is achieved at a collector current density J_C of 1×10^5 A/cm², and decreases at J_C above 2×10^5 A/cm² because of the base push-out effect (Kirk effect) at high current. According to the discussion in chapter

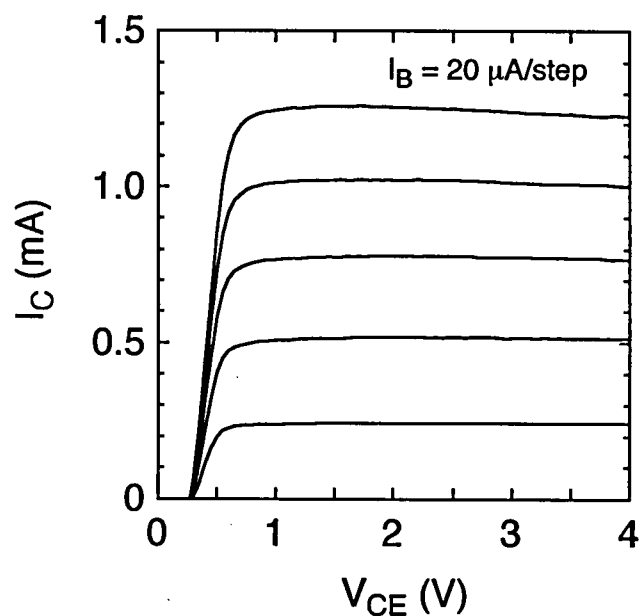


Fig. 4-11. Common-emitter $I_C - V_{CE}$ characteristics of fabricated HBT with emitter size S_E of $0.3 \mu\text{m} \times 1.6 \mu\text{m}$.

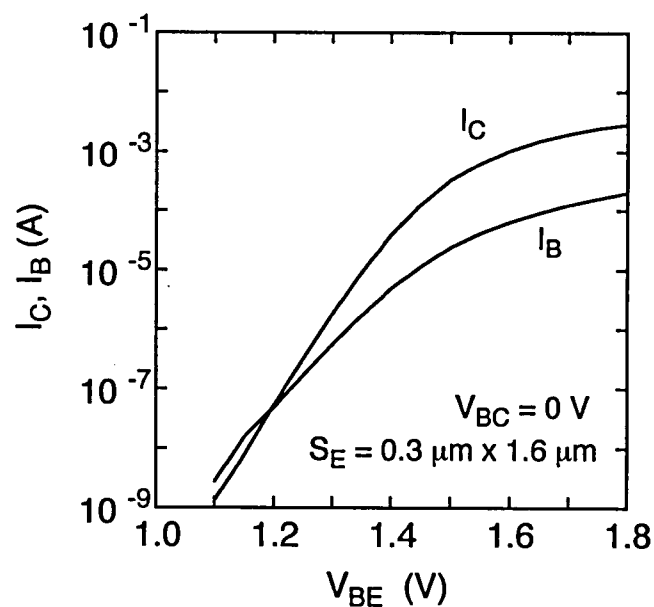


Fig. 4-12. Gummel plot for fabricated HBT with emitter size S_E of $0.3 \mu\text{m} \times 1.6 \mu\text{m}$.

3, the current gain of HBTs with the base thickness of 30 nm and the base concentration of $1.3 \times 10^{20} \text{ cm}^{-3}$ is estimated to be about 30. Therefore, the current gain of the developed HBT is smaller than the expected value.

In order to investigate the emitter size effect of the developed HBTs, the dependence of current gain h_{FE} on the ratio of the length of the emitter periphery L_E and the emitter size S_E was evaluated by using the method stated in chapter 2. Figure 4-13 shows the dependence of $1/h_{FE}$ on L_E/S_E for the developed HBTs at a collector current density of $5 \times 10^4 \text{ A/cm}^2$. Although the current gain is slightly decreased with scaling down the emitter size, the intrinsic current gain estimated from the y -intercept in Fig. 4-13 is almost 30, which is the same as the expected value. The peripheral component of the base current, estimated from the slope of the line in Fig. 4-13, was $1.8 \times 10^{-6} \text{ A/}\mu\text{m}$. This value is comparable to that of AlGaAs/GaAs HBTs with an AlGaAs surface passivation layer even though the developed HBTs do not have a thin emitter layer on the extrinsic base regions for surface passivation [12]. These results indicate that the emitter size effect of the developed small-scaled InGaP/GaAs HBTs is insignificant owing to the low surface recombination velocity of InGaP; i.e., the current gain can be improved by the reduction in the base doping concentration.

4.5.2 High-frequency characteristics

The high-frequency characteristics of the developed HBTs were investigated by measuring s -parameters using on-wafer RF probes with an HP85107A network analyzer system and cascade microwave probes. The measurements were carried out in the frequency range of 100 MHz to 40 GHz. The pad parasitics were de-embedded using the method presented by Costa et al. [37]

Figure 4-14 shows the frequency dependence of the small-signal current gain $|h_{21}|^2$, unilateral power gain U , and maximum stable gain MSG for an HBT with an emitter size S_E of $0.6 \mu\text{m} \times 4.6 \mu\text{m}$. The collector-emitter bias voltage V_{CE} was 1.6 V and the collector current I_C was 4 mA. The f_T and f_{\max} as estimated with -20 dB/decade extrapolations from $|h_{21}|^2$ and U were 138 GHz and 275 GHz, respectively.

Figure 4-15 shows the collector current dependence of f_T and f_{\max} for the developed HBT

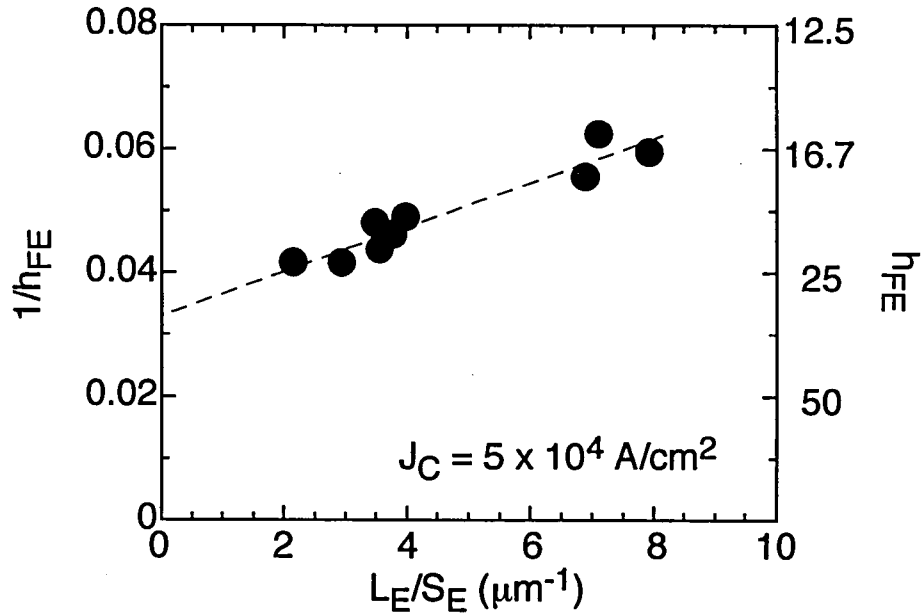


Fig. 4-13. Dependence of $1/h_{FE}$ on L_E/S_E for fabricated HBTs at collector current density J_C of $5 \times 10^4 \text{ A/cm}^2$.

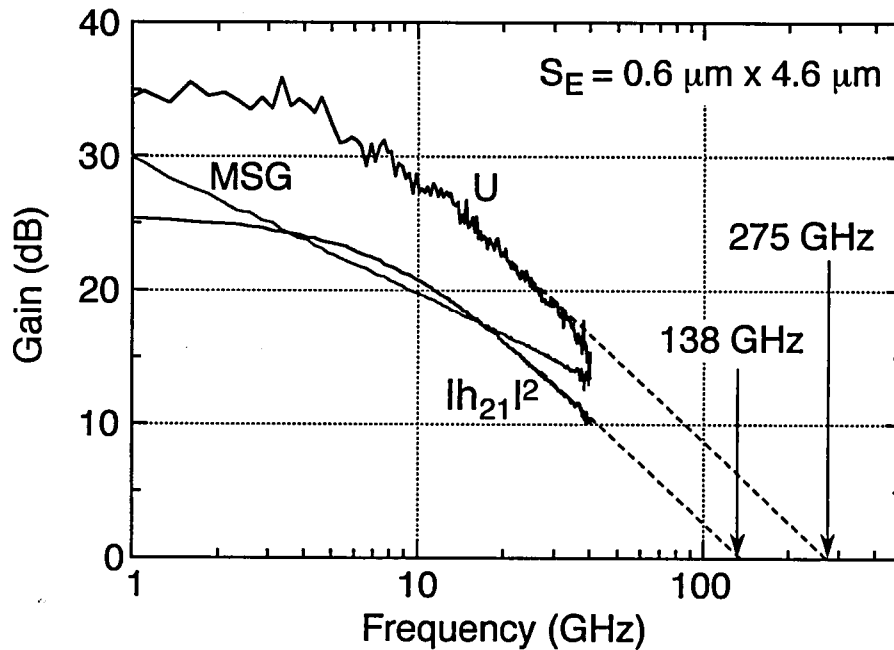
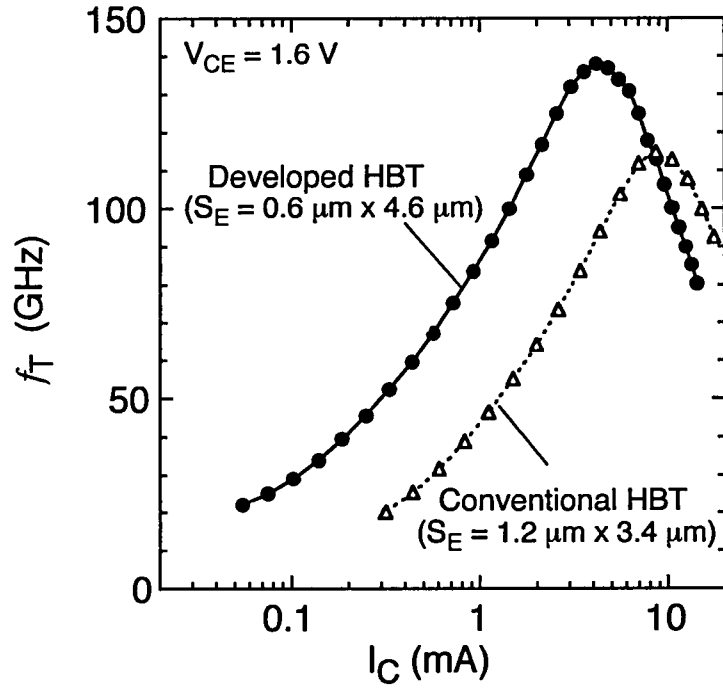
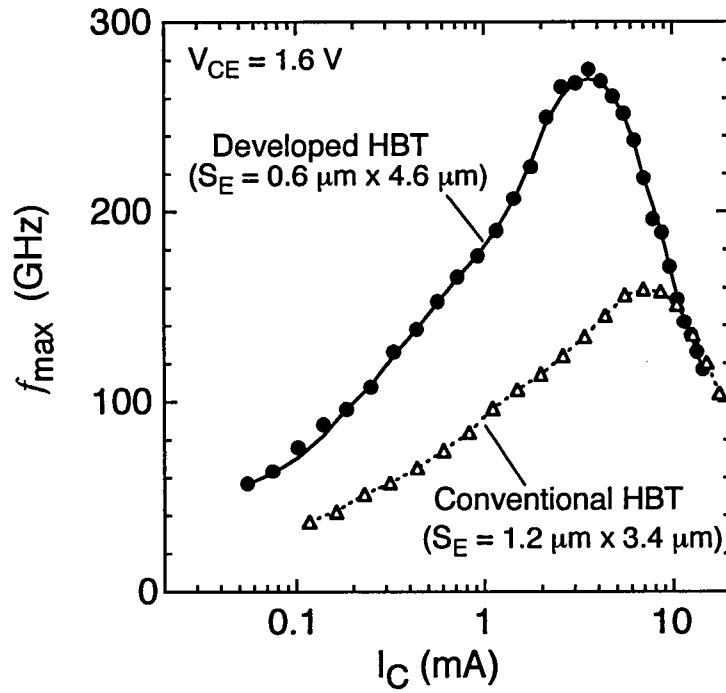


Fig. 4-14. Frequency dependence of small-signal current gain $|h_{21}|^2$, unilateral power gain U , and maximum stable gain MSG for fabricated HBT with S_E of $0.6 \mu\text{m} \times 4.6 \mu\text{m}$ at $V_{CE} = 1.6 \text{ V}$ and $I_C = 4 \text{ mA}$. The dashed lines are extrapolations of $|h_{21}|^2$ and U with a -20 dB/decade slope.



(a)



(b)

Fig. 4-15. Collector current dependence of (a) f_T and (b) f_{max} for developed HBT with S_E of $0.6 \mu\text{m} \times 4.6 \mu\text{m}$ and conventional HBT ($S_E = 1.2 \mu\text{m} \times 3.4 \mu\text{m}$) demonstrated in chapter 2.

with an S_E of $0.6 \mu\text{m} \times 4.6 \mu\text{m}$ at a V_{CE} of 1.6 V. The HBT exhibits a peak f_T of 138 GHz and a peak f_{max} of 275 GHz at an I_C of 4 mA. The figure also shows the results for the conventional HBT ($S_E = 1.2 \mu\text{m} \times 3.4 \mu\text{m}$) without using buried SiO_2 , which is demonstrated in chapter 2. The developed HBT operates at much higher f_T and f_{max} for lower collector currents than the conventional HBT. This excellent high-frequency performance for low collector currents is due to the simultaneous reduction of the emitter size and base-collector capacitance. Several characteristics of the developed HBT and the conventional HBT are summarized in Table 4-2. The C_{BC} of the developed HBT was reduced to 7.6 fF, which is about 1/3 of that of the conventional HBT, whereas the S_E of the developed HBT is about 2/3 of that of the conventional HBT. As a result, both τ_E and τ_{CC} are greatly decreased. This indicates that reducing parasitic C_{BC} with the simultaneous reduction of the emitter size effectively improves the high-frequency performance in small-scale HBTs at low collector currents. It is also shown in Fig. 4-15 that the improvement of f_T by implementing the buried SiO_2 structure is less than that of f_{max} . This is ascribed to the increase of the parasitic resistances R_{EE} and R_C resulting from the reduction of the device dimension, which increases the parasitic delay time and thus interferes the improvement of f_T . Therefore, the reduction in parasitic resistances is indispensable for the further improvement of the high-frequency performance.

Figure 4-16 shows the collector current dependence of f_T and f_{max} for the HBT with an S_E of $0.3 \mu\text{m} \times 1.6 \mu\text{m}$ at a V_{CE} of 1.6 V. The high-frequency performance is degraded compared to the larger device because the C_{BC} , the value of which is 4.1 fF, is not reduced in proportion to the emitter size. However, a peak f_T of 96 GHz and a peak f_{max} of 197 GHz are achieved at an I_C of 1 mA. Furthermore, the device exhibits f_T as high as 40 GHz and f_{max} as high as 100 GHz at an I_C as low as 0.1 mA. Compared with the results for a SiGe HBT with a small S_E of $0.14 \mu\text{m} \times 1.5 \mu\text{m}$ which exhibited high-frequency operation at a low collector current [38], the f_T and the f_{max} for the developed small HBT are higher than those for the SiGe HBT at any range of collector currents. This result indicates that the proposed HBT structure will enable the fabrication of integrated circuits with a higher speed and lower power than SiGe HBTs.

Table 4-2. Device characteristics of the developed HBT and the conventional HBT.

	Developed HBT	Conventional HBT
$S_E(\mu\text{m}^2)$	0.6 x 4.6	1.2 x 3.4
R_{EE} (Ω)	13	6.6
R_B (Ω)	26	25
R_C (Ω)	11	8.1
C_{EB} (fF)	7.0	13.8
C_{BC} (fF)	7.6	25.8
f_T (GHz)	138	115
f_{max} (GHz)	275	159

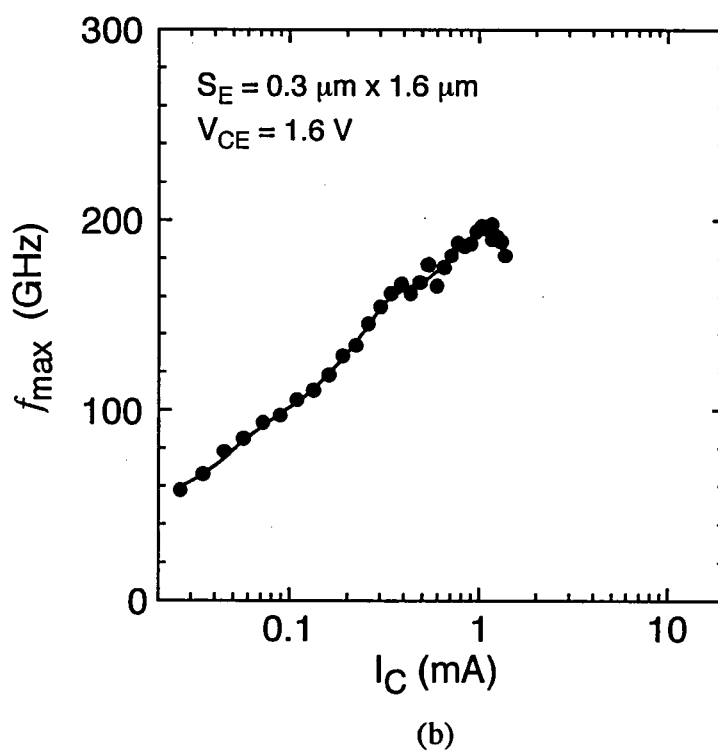
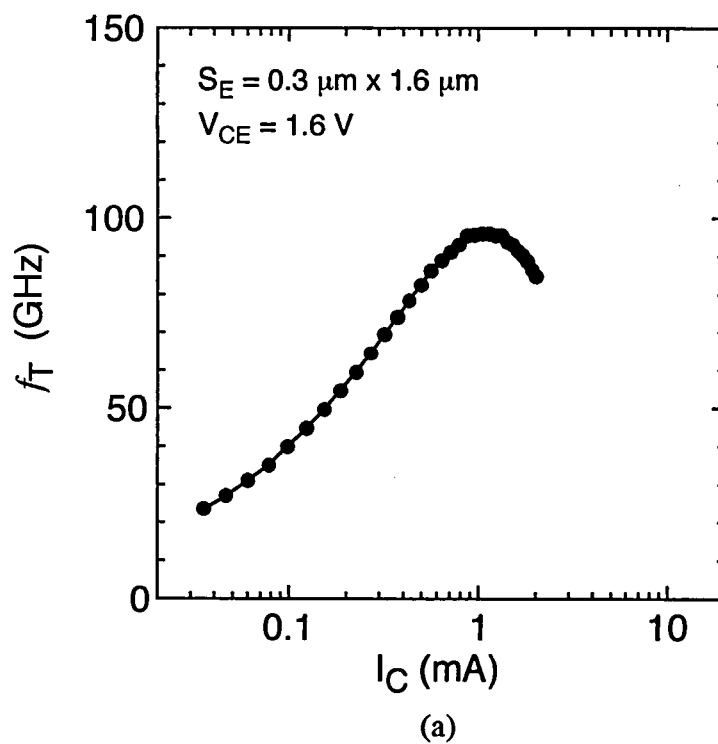


Fig. 4-16. Collector current dependence of (a) f_T and (b) f_{max} for developed HBT with S_E of $0.3 \mu\text{m} \times 1.6 \mu\text{m}$ at V_{CE} of 1.6 V.

4.6 Summary

High-speed and low-current operations of InGaP/GaAs HBTs have been demonstrated. A novel device structure with process technology was proposed to realize high-speed and low-power operation of small-scale InGaP/GaAs HBTs. The structure had a WSi/Ti base electrode and buried SiO₂ in the extrinsic collector region under the base electrode, those enabled the simultaneous reduction of both the emitter size and the parasitic base-collector capacitance.

The ohmic contact characteristics of WSi/Ti metals were investigated to utilize them as the base electrode. The specific contact resistance ρ_c of WSi for *p*-GaAs with an N_B of $1 \times 10^{20} \text{ cm}^{-3}$ was dramatically reduced from $2 \times 10^{-6} \Omega \cdot \text{cm}^2$ to $3 \times 10^{-7} \Omega \cdot \text{cm}^2$ by inserting a 5-nm Ti film between the interface. The low ρ_c made it possible to reduce the optimum base contact width for achieving both high f_T and high f_{\max} to less than $0.4 \mu\text{m}$ without the large increase in the base resistance. The fabricated device structure exhibited that the WSi/Ti base electrode covered both the narrow base contact surface and the buried SiO₂ outside of the base-collector junction, indicating that WSi and Ti are useful metals in fabricating the base electrodes for small-scale HBTs with a narrow contact region and buried SiO₂.

Utilizing an InGaP emitter effectively suppressed the emitter size effect and, as a result, a DC current gain of 20 was achieved for an HBT with an S_E of $0.3 \mu\text{m} \times 1.6 \mu\text{m}$. Small-scale devices demonstrated excellent high-frequency characteristics at low collector currents: an HBT with an S_E of $0.6 \mu\text{m} \times 4.6 \mu\text{m}$ provided an f_T of 138 GHz and an f_{\max} of 275 GHz at an I_C of 4 mA; and an HBT with an S_E of $0.3 \mu\text{m} \times 1.6 \mu\text{m}$ provided an f_T of 96 GHz and an f_{\max} of 197 GHz at an I_C of 1 mA. The higher speed and lower current operations of the developed HBTs than those of conventional HBTs verified that the simultaneous reduction of both the emitter size and the extrinsic collector capacitance was effective for improving the high-frequency performance in small-scale GaAs HBTs, indicating the great potential of the proposed HBT structure for high-speed and low-power applications.

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Chapter 5

Improvement of High-Frequency Performance in Small-Scale InGaP/GaAs HBTs and Their Applications to Integrated Circuits

5.1 Introduction

In chapter 4, a novel device structure of an HBT with a WSi/Ti base electrode and buried SiO₂ in the extrinsic collector was proposed. This novel device structure enabled simultaneous reduction in both the emitter size and the base-collector parasitic capacitance and, thus, allowed the developed GaAs HBTs to operate at a high frequency and a low collector current compared to conventional GaAs HBTs. Among the developed HBTs, however, the high-frequency performance of smaller devices was degraded compared to that of larger devices. The reason is explained by Fig. 5-1. Figure 5-1 shows the dependence of the emitter resistance R_{EE} and the base-collector capacitance C_{BC} on the emitter size of the developed HBTs demonstrated in chapter 4. The emitter resistance is reversely proportional to the emitter size; while the capacitance is not scaled down in proportion to the emitter size because of the parasitic capacitance, as shown in Fig. 5-1(b). This implies that the parasitic capacitance still influences the increase in parasitic delays even though the extrinsic capacitance was substantially reduced compared to the conventional devices.

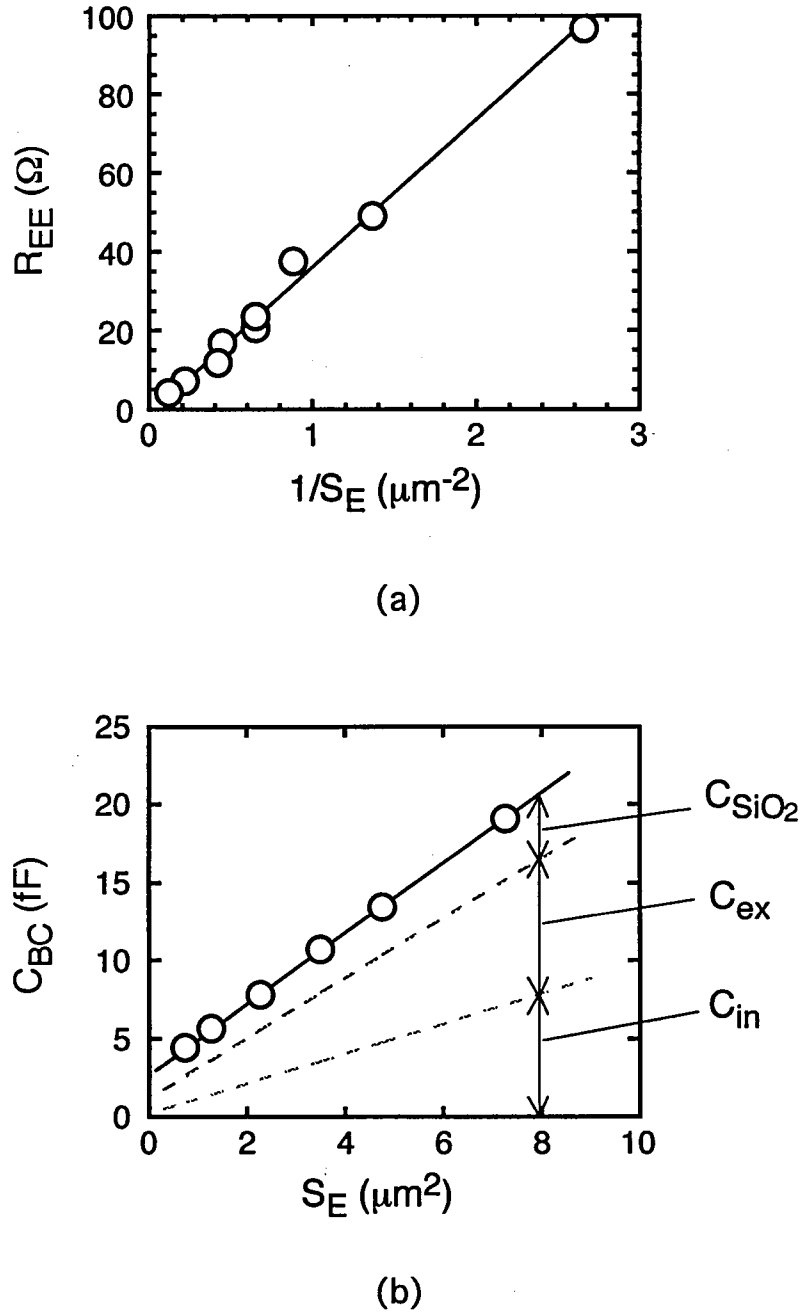


Fig. 5-1. Dependence of (a) emitter resistance R_{EE} and (b) base-collector capacitance C_{BC} on emitter size S_E for the developed HBTs demonstrated in chapter 4. The components of the intrinsic and extrinsic capacitances (C_{in} and C_{ex}) at the base-collector junction region and the parasitic capacitance (C_{SiO_2}) at the buried SiO_2 region - calculated according to their areas - are also shown.

In this chapter, the advanced high-frequency performance of small-scale InGaP/GaAs HBTs is exhibited. To improve the high-frequency characteristics of small-scale devices, the base-collector capacitance is further reduced by refining the process technology and the device design. The characteristics of the improved HBTs are compared with the previously-reported high-performance bipolar devices. The capability of the developed HBTs for high-speed and low-power integrated circuits is also investigated by applying them to 1/8 static frequency dividers as digital circuits and transimpedance amplifiers as analog circuits.

5.2 Refinements of Fabrication Process

For the further reduction of the parasitic C_{BC} caused by a buried SiO_2 , C_{SiO_2} , the fabrication process was refined to increase the thickness of the buried SiO_2 and to reduce the area of the base electrode.

With respect to the buried SiO_2 thickness, the thickness was limited by the uneven surface after planarization. Figure 5-2 shows the schematic illustrations of the planarized surface before and after etchback. The flatness of planarized surface depends on the layout patterns, giving rise to the uneven surface. This causes the non-uniformity of the buried SiO_2 thickness after etchback, which makes it difficult to bury thick SiO_2 , as well as lowers the device yield.

To improve the flatness of the planarized surface, a double photoresist coating with high-temperature reflow was proposed. Figure 5-3 shows the SEM cross-sections at the first photoresist coating before and after reflow. The surface flatness was considerably improved by the high-temperature reflow over 200°C. Together with the second photoresist coating, the flatness of the planarized surface was further improved; that is, the variation of the thickness of the buried SiO_2 in a 3-inch-diameter wafer after etchback was reduced from over 100 nm to below 40 nm. In consequence, the thickness of the buried SiO_2 was successfully increased to 0.5 μm , which is 25% larger than that in the previous process used in chapter 4, as well as the device yield from 70% to more than 90%.

In regard to the area reduction of the base electrode, dry-etching process of WSi metal

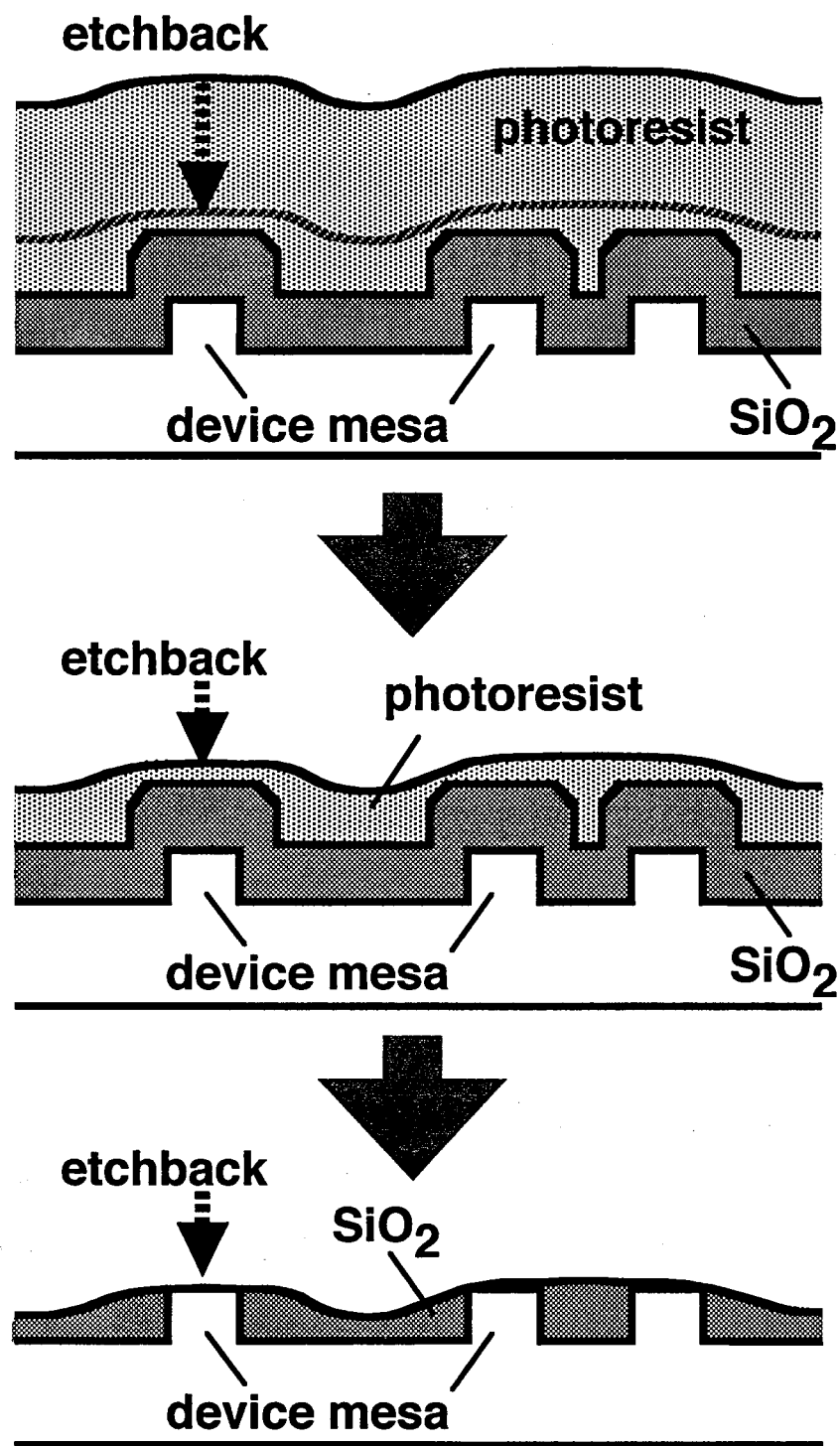
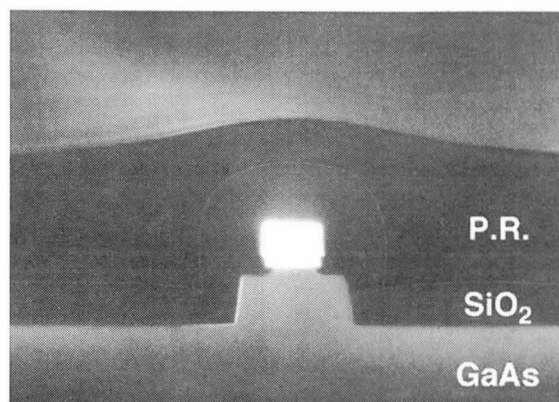
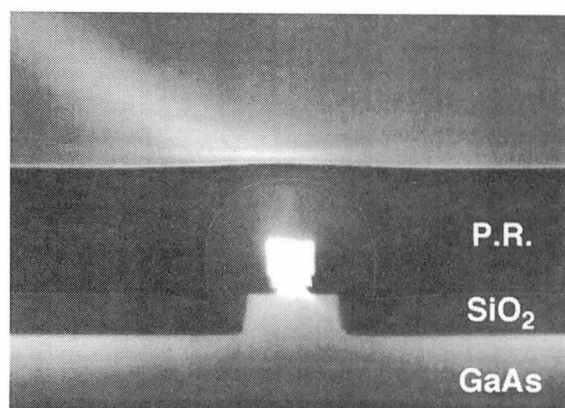


Fig. 5-2. Schematic illustrations of the planarized surface before and after etchback. Layout patterns give rise to the unevenness of the planarized surface, causing the non-uniformity of the SiO₂ thickness after etchback.



(a)



(b)

Fig. 5-3. SEM cross-sections at the first photoresist coating (a) before and (b) after reflow at 200°C.

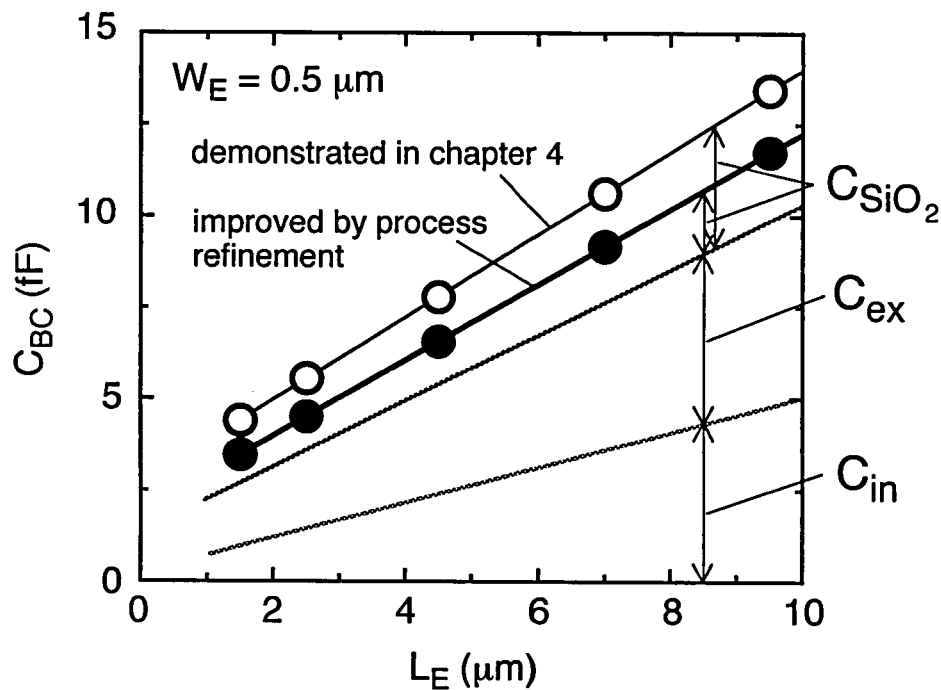


Fig. 5-4. Emitter length dependence of the base-collector capacitance C_{BC} at a zero bias with an emitter width W_E of $0.5 \mu\text{m}$. The solid and open circles, respectively, represent the improved HBTs by process refinement and the developed HBTs demonstrated in chapter 4. The components of the intrinsic and extrinsic capacitances (C_{in} and C_{ex}) at the base-collector junction region and the parasitic capacitance (C_{SiO_2}) at the buried SiO_2 region - calculated according to their areas - are also shown.

was refined. An isotropic etching with high etching selectivity between WSi and SiO₂ was accomplished by a chemical dry etching by CF₄ radicals. This enabled the reduction of the base electrode area by controlling the side-etching time. Consequently, the electrode area was reduced by about 20% compared to the previous devices stated in chapter 4.

Figure 5-4 shows the emitter length dependence of base-collector capacitance C_{BC} of the HBTs with an emitter width of 0.5 μm fabricated by using the refined processes and the previous process demonstrated in chapter 4. In the figure, the components of the intrinsic and extrinsic capacitances (C_{in} and C_{ex}) at the base-collector junction region and the parasitic capacitance (C_{SiO_2}) at the buried SiO₂ region — calculated according to their areas — are also shown for comparison. It is signified that, by the process refinements, the parasitic capacitance at the buried SiO₂ region is reduced by 50% compared to the previous devices. The reduction of the capacitance is more effective in smaller devices. For instance, C_{BC} of a device with an emitter-length of 9.5 μm is reduced by 13%, while C_{BC} of a device with an emitter-length of 1.5 μm is reduced by 21%. This result suggests that the process refinements will bring further improvement of high-frequency performance in small-scale GaAs HBTs.

5.3 Device Fabrication

The parameters of the epitaxial layer structure are listed in Table 5-1. The layer structure is the same as that used in chapter 4 except for the base doping concentration. To obtain a higher current gain than that in chapter 4, the doping concentration was reduced to $1 \times 10^{20} \text{ cm}^{-3}$.

The device fabrication process is basically the same as that described in chapter 4. The refined processes were utilized for the planarization and the dry etching of WSi. The width of the base contact region was optimized for attaining both high f_T and high f_{max} . When the base doping concentration was $1 \times 10^{20} \text{ cm}^{-3}$ and the buried SiO₂ thickness was 0.5 μm for the device with an emitter size of 0.5 $\mu\text{m} \times 5 \mu\text{m}$, the optimum W_{BC} for obtaining the minimum value of the product of R_B and C_{BC} was calculated to be 0.25 μm . Therefore, W_{BC} was designed as 0.25 μm by controlling the thickness of SiO₂ sidewalls for the self-align mask of the

Table 5-1. Parameters of epitaxial layer structure of fabricated HBTs.

Layer	Material	Doping Concentration (cm ⁻³)	Thickness (nm)
Emitter-cap	<i>n</i> -InGaAs	4×10^{19}	50
	<i>n</i> -GaAs	8×10^{18}	100
	<i>n</i> -InGaP	8×10^{18}	50
Emitter	<i>n</i> -InGaP	5×10^{17}	100
Base	<i>p</i> -GaAs	1×10^{20}	30
Collector	<i>n</i> -GaAs	2×10^{16}	200
Subcollector	<i>n</i> -GaAs	8×10^{18}	800

base-collector mesa formation and for the emitter-base separation.

The process for wiring to fabricate integrated circuits is as follows. After devices are passivated and planarized with SiO₂ and spin-on-glass, as shown in Fig. 4-9(h) in chapter 4, WSiN resistors with 100 Ω /square sheet resistance and the first level of the metallization are fabricated. This metallization forms most of the probe pads, resistor contacts, capacitor bottom plate, interconnect wiring, and transmission lines. To serve as interconnect crossovers for the second wiring levels, the first level of metallization is passivated and planarized with SiO₂ and spin-on-glass. SiN is then deposited and etched away in unwanted regions in order to form MIM capacitors. Finally, Au is evaporated to form the second level of metallization and the top plate of the MIM capacitors.

5.4 Device Performance

5.4.1 DC characteristics

DC characteristics of an improved HBT with an emitter size S_E of $0.25 \mu\text{m} \times 1.5 \mu\text{m}$ are shown in Fig. 5-5. Figure 5-5(a) shows the common-emitter $I_C - V_{CE}$ characteristics. A small signal current gain h_{fe} of 28 is attained. The offset voltage is about 0.3 V, and the collector-emitter breakdown voltage BV_{CEO} is 9.6 V. Figure 5-5(b) shows a Gummel plot at a base-collector bias voltage V_{BC} of 0 V. The DC current gain h_{FE} of 30 is achieved at a collector current density J_C of $1 \times 10^5 \text{ A/cm}^2$. The gain is about 1.5 times larger than that of the HBT demonstrated in chapter 4, resulting from the decrease in the base doping concentration.

5.4.2 High-frequency characteristics

Figure 5-6 shows the frequency dependence of small-signal current gain $|h_{21}|^2$, unilateral power gain U , and maximum stable gain MSG for an HBT with an S_E of $0.5 \mu\text{m} \times 4.5 \mu\text{m}$. The collector-emitter bias voltage V_{CE} was 1.5 V and the collector current I_C was 3.5 mA. The f_T and f_{max} as estimated with -20 dB/decade extrapolations from $|h_{21}|^2$ and U were

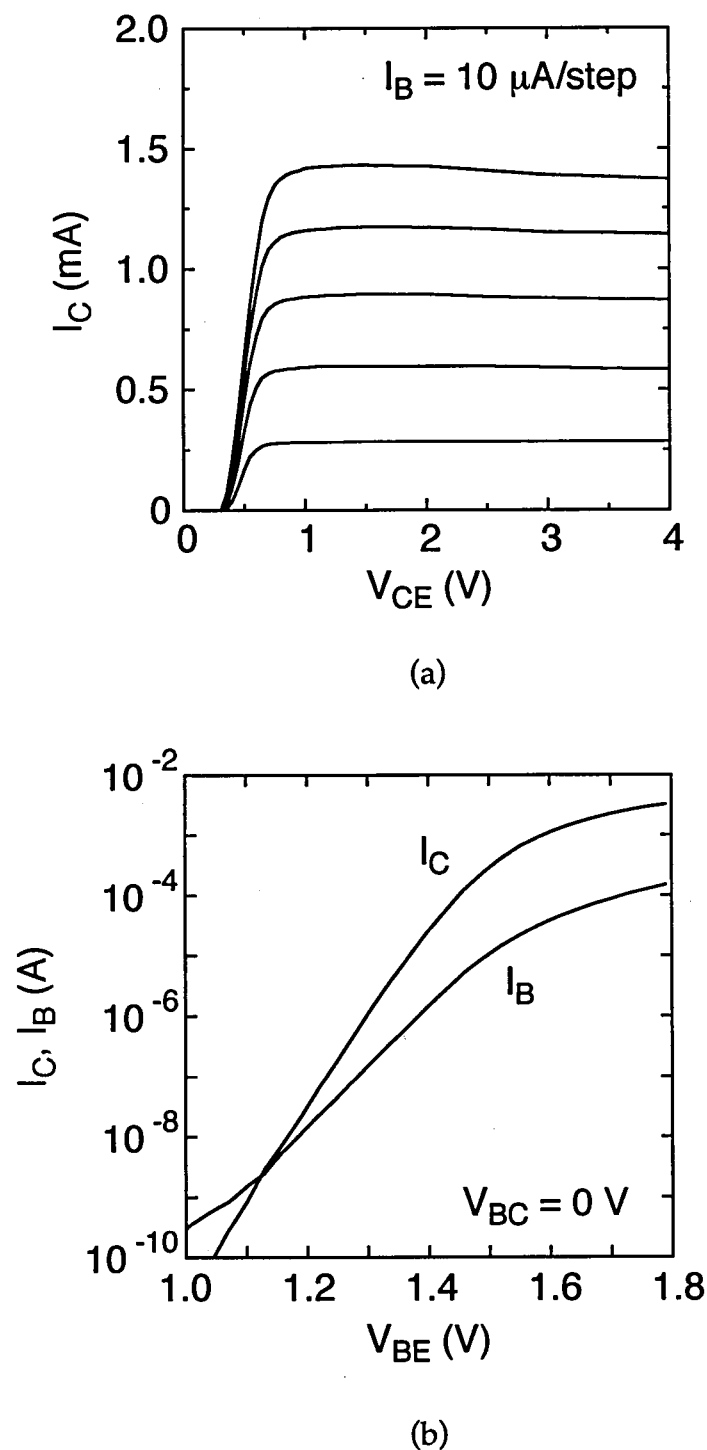


Fig. 5-5. DC characteristics for improved HBT with an emitter size S_E of $0.25 \mu\text{m} \times 1.5 \mu\text{m}$: (a) common-emitter $I_C - V_{CE}$ characteristics; (b) Gummel plot.

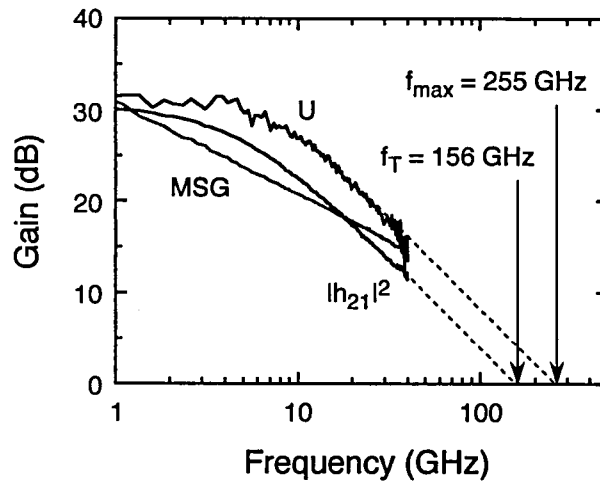


Fig. 5-6. Frequency dependence of small-signal current gain $|h_{21}|^2$, unilateral power gain U , and maximum stable gain MSG of improved HBT with S_E of $0.5 \mu\text{m} \times 4.5 \mu\text{m}$. The measurements were done at $V_{CE} = 1.5 \text{ V}$ and $I_C = 3.5 \text{ mA}$. The dashed lines are extrapolations of $|h_{21}|^2$ and U with a -20 dB/decade slope.

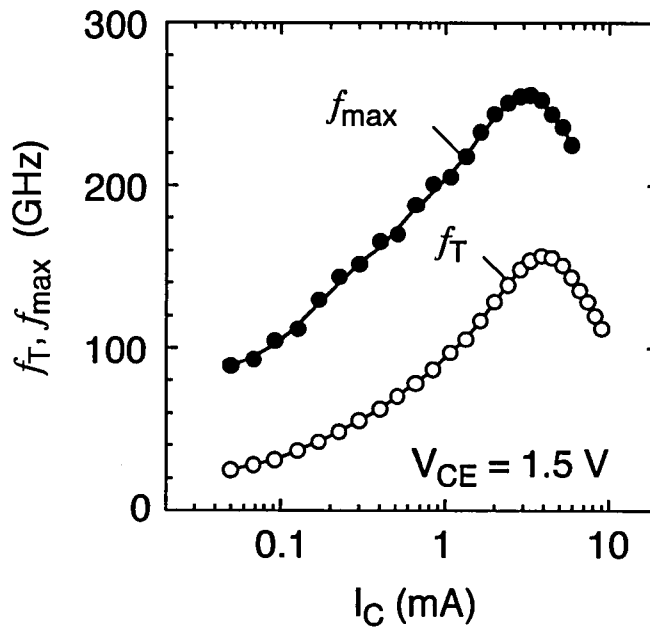


Fig. 5-7. Dependence of f_T and f_{max} on collector current of improved HBT with S_E of $0.5 \mu\text{m} \times 4.5 \mu\text{m}$ measured at $V_{CE} = 1.5 \text{ V}$.

156 GHz and 255 GHz, respectively. Figure 5-7 shows the dependence of f_T and f_{\max} on I_C of the HBT with an S_E of $0.5 \mu\text{m} \times 4.5 \mu\text{m}$ at a V_{CE} of 1.5 V. The HBT exhibits a peak f_T of 156 GHz at an I_C of 3.5 mA and a peak f_{\max} of 260 GHz at an I_C of 3.2 mA. The f_{\max} is lower than that of the HBT demonstrated in chapter 4. This is ascribed to the reduction of both the base doping concentration and the base contact width, those increased the base resistance. In contrast, the f_T is increased by 18 GHz owing to the further reduction of the parasitic capacitance. To the author's knowledge, this is the first result of GaAs HBTs with f_T over 150 GHz and f_{\max} over 250 GHz.

Figure 5-8 shows the frequency dependence of $|h_{21}|^2$, U , and MSG for an HBT with an S_E of $0.25 \mu\text{m} \times 1.5 \mu\text{m}$ at a V_{CE} of 1.5 V and an I_C of 0.9 mA. The estimated f_T and f_{\max} were 114 GHz and 230 GHz, respectively. Figure 5-9 shows the dependence of f_T and f_{\max} on I_C of the HBT with an S_E of $0.25 \mu\text{m} \times 1.5 \mu\text{m}$ at a V_{CE} of 1.5 V. A peak f_T of 114 GHz and a peak f_{\max} of 230 GHz are achieved at an I_C of only 0.9 mA. Furthermore, the device operates at f_T as high as 50 GHz and f_{\max} as high as 135 GHz at an I_C as low as 0.1 mA. These excellent high-frequency characteristics at the low collector currents are due to the simultaneous reduction of the emitter size and base-collector capacitance. Typical device characteristics of the improved HBTs are summarized in Table 5-2.

Figure 5-10 compares the dependence of peak f_T and peak f_{\max} on S_E of the improved HBTs with the devices demonstrated in chapter 4. The improved HBTs exhibited much better high-frequency performance with a much smaller emitter size than HBTs demonstrated in chapter 4, indicating that further reduction of the parasitic C_{BC} by the process and design refinements effectively suppresses the degradation of high-frequency performance in small-scale devices.

Here the performance of the developed HBTs are compared with those of previously-reported high-performance HBTs. Figure 5-11 shows the comparison of dependence of peak f_T and peak f_{\max} on I_C [1-22]. The developed HBTs operate at higher frequency for low collector currents than not only previously-reported GaAs HBTs, but also SiGe and InP HBTs. Figure 5-12 compares f_T and BV_{CEO} of the developed HBTs with previously-reported high-speed HBTs [4-14,18-22]. The $f_T - BV_{CEO}$ product is one of the figures-of-merits of high-speed bipolar devices because the BV_{CEO} can be traded off for f_T related to the collector thickness. The

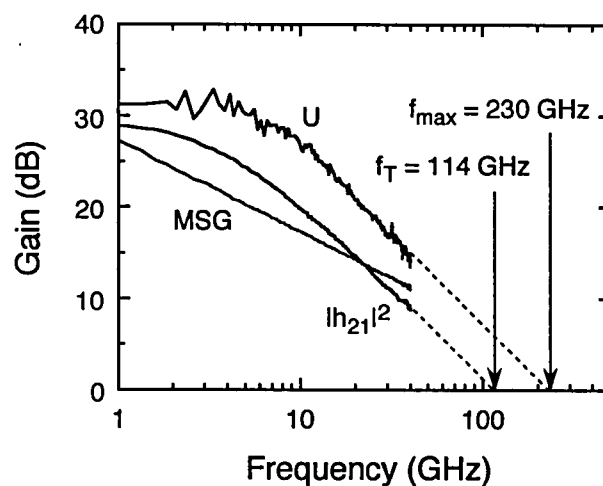


Fig. 5-8. Frequency dependence of small-signal current gain $|h_{21}|^2$, unilateral power gain U , and maximum stable gain MSG of improved HBT with S_E of $0.25 \mu\text{m} \times 1.5 \mu\text{m}$ measured at $V_{CE} = 1.5 \text{ V}$ and $I_C = 0.9 \text{ mA}$.

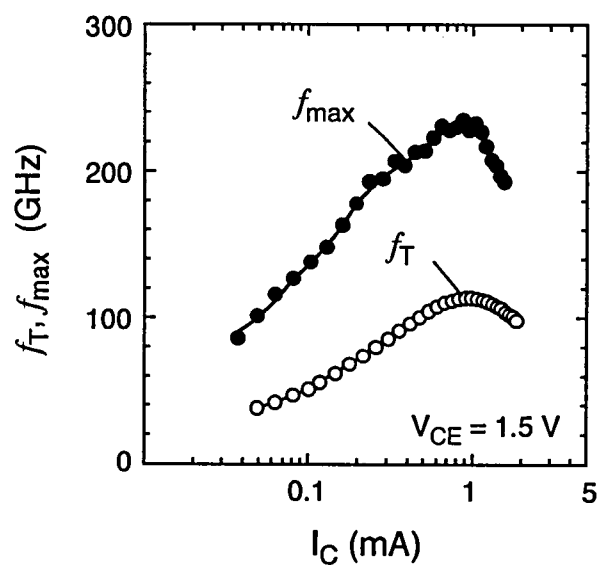


Fig. 5-9. Dependence of f_T and f_{max} on collector current of improved HBT with S_E of $0.25 \mu\text{m} \times 1.5 \mu\text{m}$ measured at $V_{CE} = 1.5 \text{ V}$.

Table 5-2. Device characteristics of improved HBTs.

Emitter size (μm^2)	0.5 x 4.5	0.25 x 1.5
$h_{FE_{\max}}$	35	30
BV_{CEO} (V)	9.6	9.6
Emitter resistance (Ω)	15	90
Base resistance (Ω)	29	53
Collector resistance (Ω)	6.3	11
Emitter capacitance (fF)	6.2	1.8
Collector capacitance (fF)	6.7	3.5
peak f_T (GHz)	156	114
peak f_{\max} (GHz)	255	230
Emitter charging time (ps)	0.23	0.39
Intrinsic transit time (ps)	0.65	0.65
Collector charging time (ps)	0.14	0.35

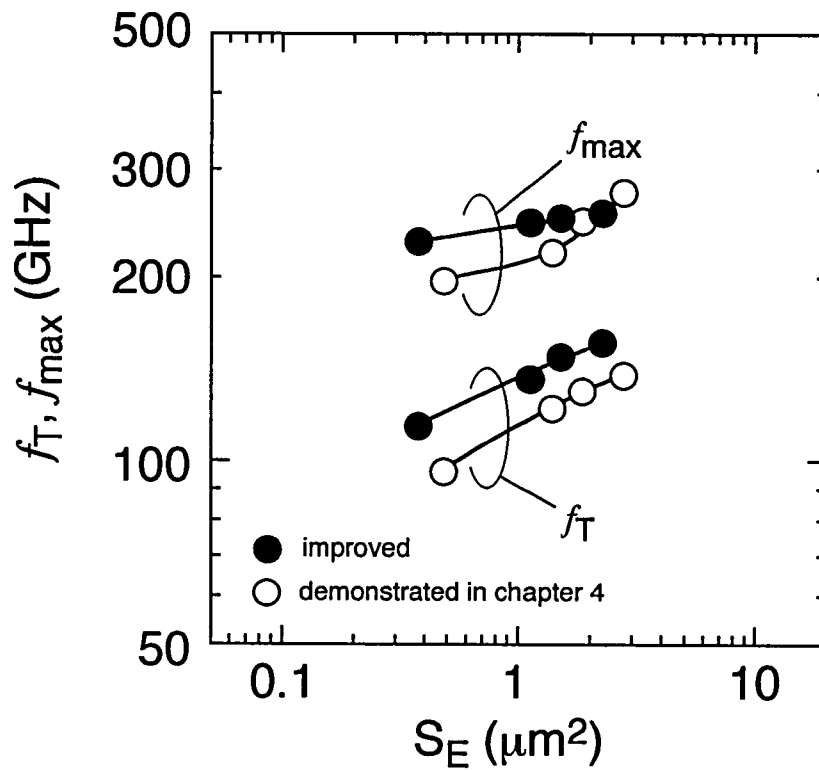
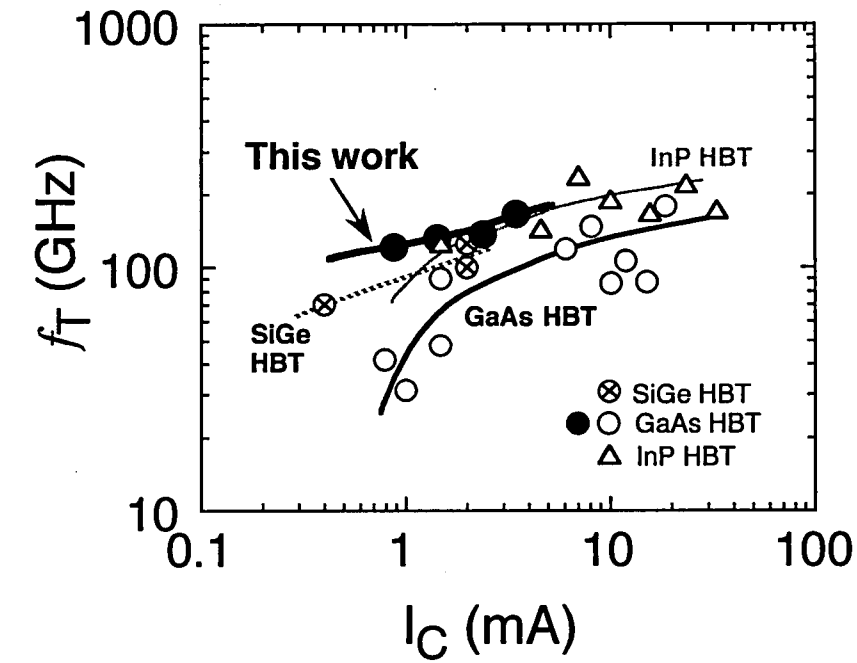
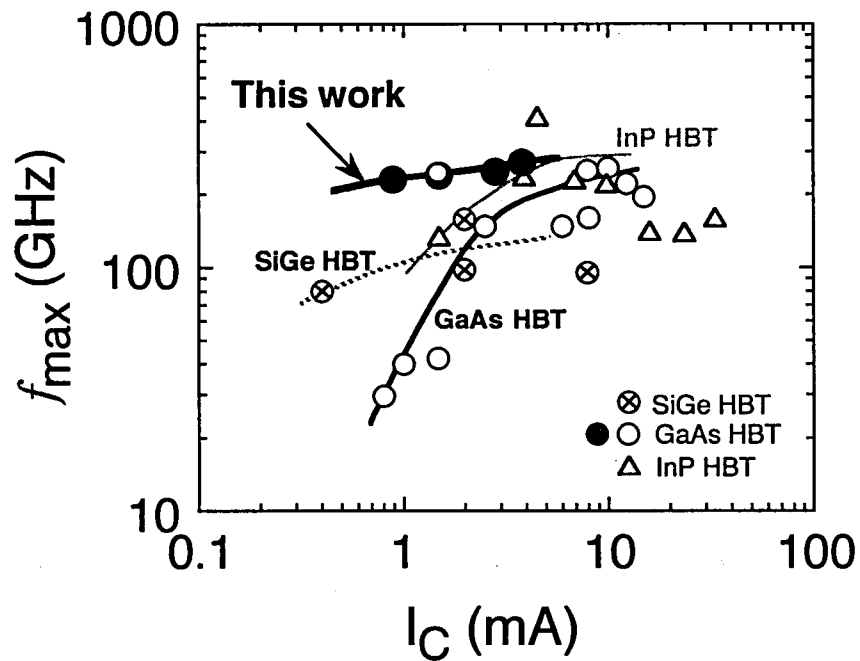


Fig. 5-10. Comparison of the peak f_T and peak f_{max} versus emitter size S_E of improved HBTs with the HBTs demonstrated in chapter 4.



(a)



(b)

Fig. 5-11. Comparison of dependence of (a) peak f_T and (b) peak f_{max} on collector currents I_C of improved HBTs with previously reported high-performance HBTs.

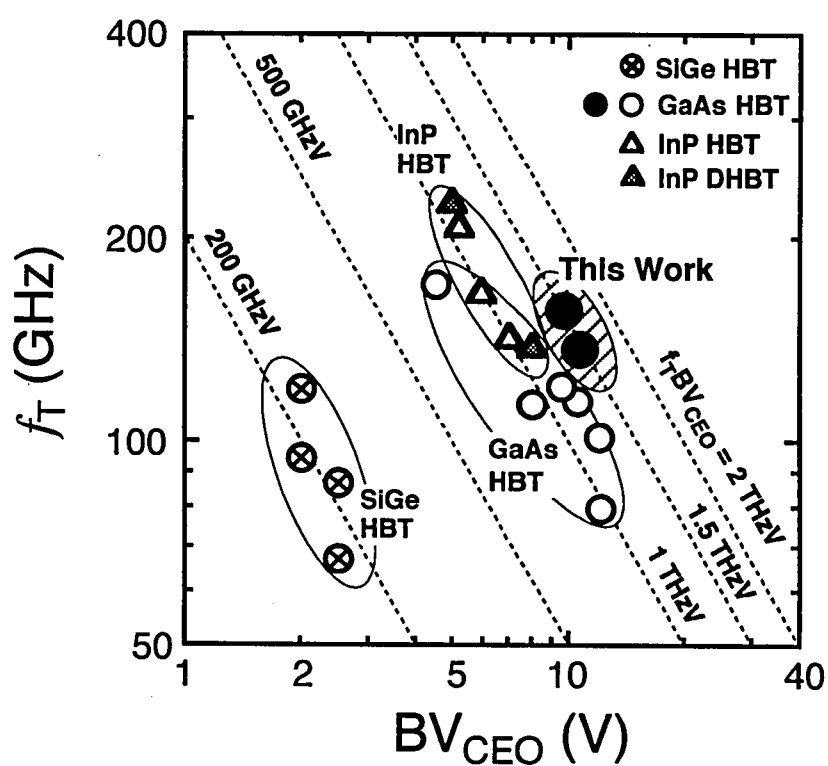


Fig. 5-12. Comparison of f_T and BV_{CEO} of improved HBTs with previously reported high-speed HBTs.

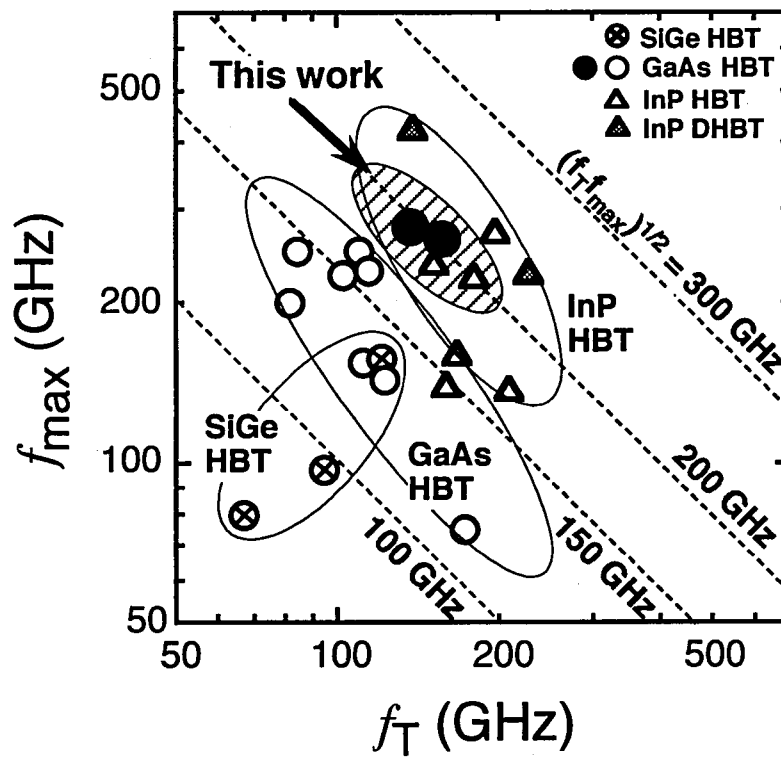


Fig. 5-13. Comparison of f_T and f_{max} of improved HBTs with previously reported high-speed HBTs.

developed HBTs achieve the highest $f_T - BV_{CEO}$ product of 1.5 THz·V, suggesting the potential of the developed HBTs for both ultra-high-speed digital ICs and analog ICs with large output voltages. Furthermore, the value is even larger than that of InP double heterojunction bipolar transistors (DHBTs) [13,18]. This implies that, by optimizing the collector thickness, the developed HBTs can operate at higher frequency than InP DHBTs for a given breakdown voltage. Figure 5-13 shows the comparison of the values of the f_T/f_{max} pair with those of previously reported high-speed HBTs [4-14,18-22]. The f_T/f_{max} pair is also one of the figures-of-merits for high-speed digital and analog circuits [23]. The developed HBTs exhibit the highest f_T/f_{max} pair among the GaAs HBTs ever reported. It should be noted that, although some InP HBTs demonstrated much higher performance, the developed HBTs exhibit the high values at lower collector currents than InP HBTs, as shown in Fig. 5-11. These results indicate a great potential of the developed HBTs for high-speed and low-power operations.

5.5 Applications to Integrated Circuits

To investigate the capability of the developed HBTs as elements of high-speed and low-power integrated circuits, the developed technology was applied to the fabrication of 1/8 static frequency dividers as digital circuits and transimpedance amplifiers as analog circuits.

5.5.1 Static frequency divider

A block diagram of a 1/8 static frequency divider is shown in Fig. 5-14. The frequency divider consists of an input buffer composed by emitter followers with 50-Ω on-chip resistors, three stages of divide-by-two master-slave T-type flip-flop (MS-T-FF) with an internal buffer in series, and an output buffer consisting of a differential amplifier. Figure 5-15 shows the circuit diagram of MS-T-FF. Each T-FF is constructed with series-gated emitter-coupled logic (ECL) with an internal single-ended voltage swing of 400 mV. The divider includes 187 transistors with an S_E of $0.5 \mu\text{m} \times 4.5 \mu\text{m}$. Some diodes are inserted in order to control the bias of the HBTs around the peak f_T and f_{max} . The supply voltages V_{EE} and V_{CS} are -6.5 V and -2.0 V,

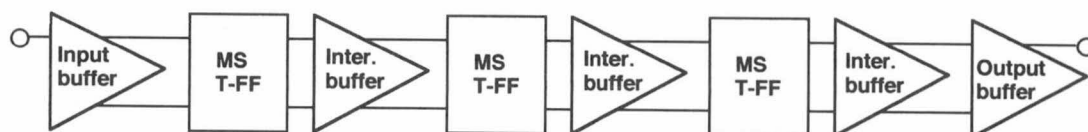


Fig. 5-14. Block diagram of a 1/8 static frequency divider.

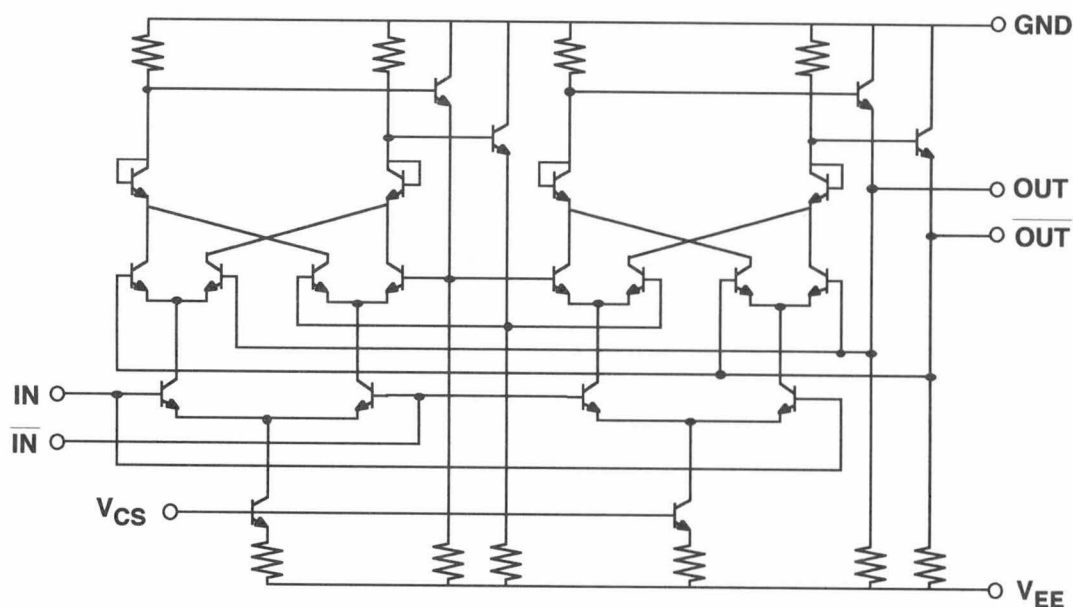


Fig. 5-15. Circuit diagram of master-slave T-type flip-flop.

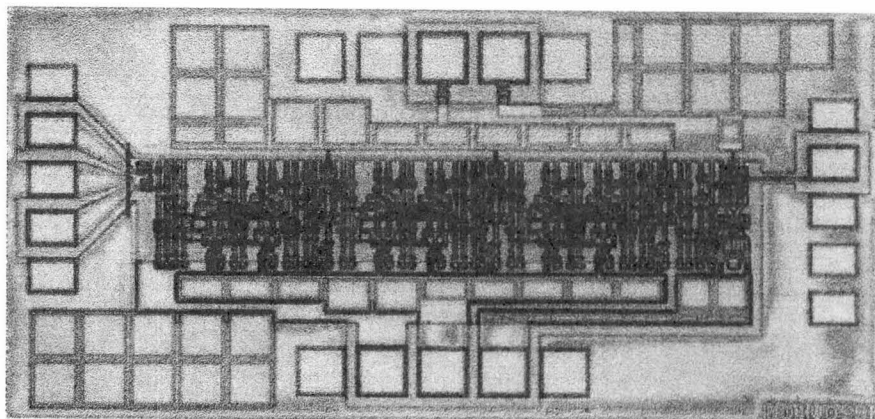


Fig. 5-16. Chip micrograph of the frequency divider.

respectively, and the collector current per ECL transistor tree is 4.8 mA. Although the operating current density was rather high ($J_C \sim 2 \times 10^5$ A/cm²), significant degradations of characteristics were not observed during the operations. Figure 5-16 shows a chip micrograph of the fabricated frequency divider. The size of the chip is 0.9 mm \times 1.8 mm and the MS-T-FF with the internal buffer occupies 210 μ m \times 440 μ m. About 1/3 of the chip area is filled with large capacitors, so-called decoupling capacitors, which are inserted between the each power supply line and the ground in order to stabilize the supply voltages.

The measured minimum input peak-to-peak voltage V_{p-p} versus the input frequency of the fabricated divider is shown in Fig. 5-17. The divider was driven by a single-ended input signal, and reliable operation was guaranteed above the minimum input voltage. In the frequency range of 3-38 GHz, the minimum input voltage is less than 500 mV_{p-p}. The self-oscillation frequency is about 24 GHz, and the divider operates up to 39.5 GHz. Figure 5-18 shows the input and output waveforms at the highest frequency operation. The power consumption per flip-flop is 190 mW.

Figure 5-19 shows the dependence of the maximum toggle frequency on the power per flip-flop. The results for previously-reported static frequency dividers using ECL gates are also shown in the figure [10,19,20,24-27]. The power consumption of the fabricated dividers is about 2/3 of those of previously-reported GaAs-HBT static frequency dividers with the same operating frequency [10,24]. This result verifies that the simultaneous reduction of both the emitter size and the parasitic C_{BC} is effective for the high-speed and low-power operation of digital circuits. Although higher frequency operation is achieved by InP HBTs due to the higher f_T , the power consumption is further high because of the larger S_E . Since the developed GaAs HBTs had higher $f_T - BV_{CEO}$ product than InP HBTs, as shown in Fig. 5-12, the optimization of the collector thickness for a given breakdown voltage will enable the developed HBTs to operate with much higher toggle frequency at the same power than InP HBTs. It should be noted that the maximum toggle frequency for SiGe HBTs is higher than that for the developed GaAs HBTs in spite of the lower f_T and f_{max} of the SiGe HBTs [20]. This is probably ascribed to interconnect delay owing to the relatively relaxed circuit layout, as shown in Fig. 5-16. Therefore, the refinement of the layout design for wiring is the key issue for the improvement in the high-frequency operation of digital circuits using the developed

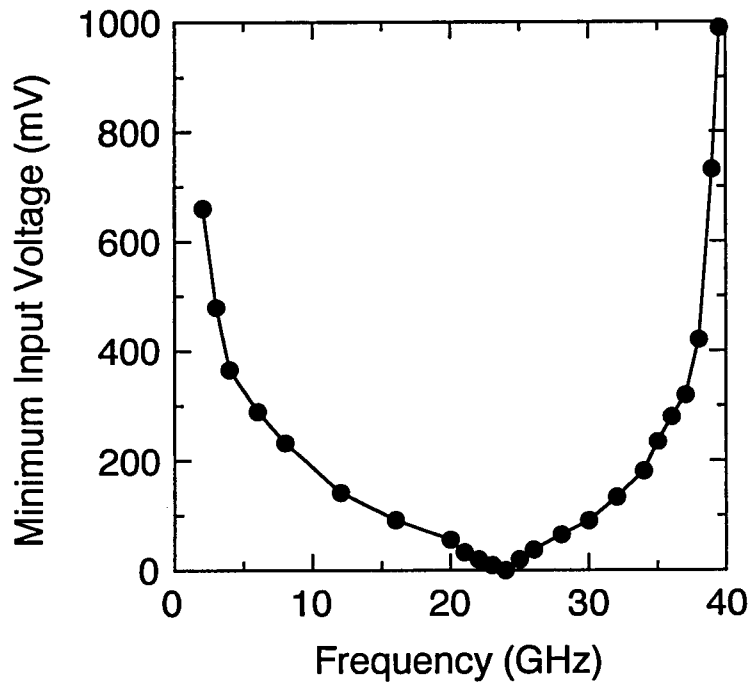


Fig. 5-17. Measured minimum input voltage V_{p-p} versus input frequency of the divider.

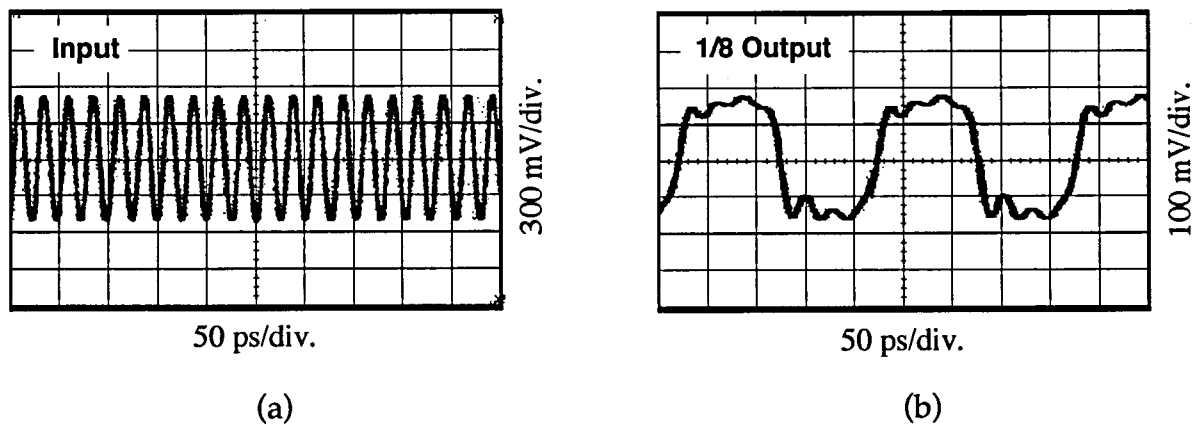


Fig. 5-18. Measured (a) input and (b) output waveforms of the 1/8 static frequency divider at 39.5 GHz.

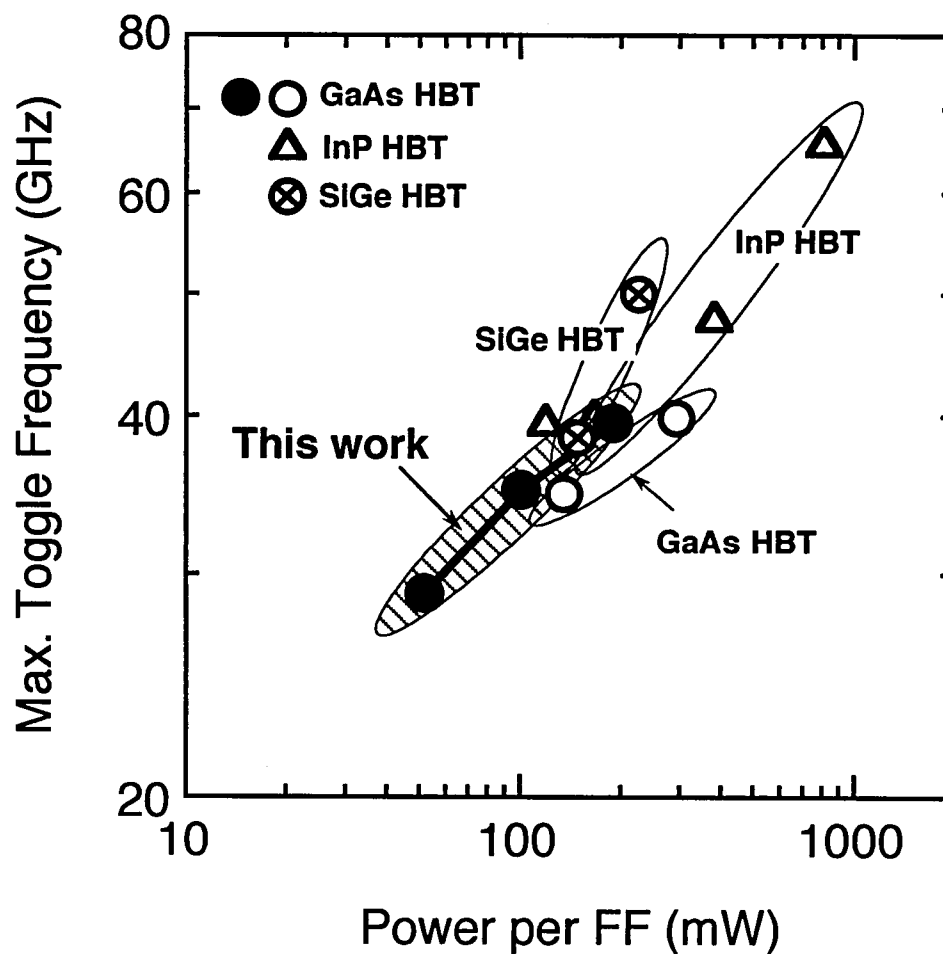


Fig. 5-19. Comparison of dependence of the maximum toggle frequency on the power per flip-flop of fabricated frequency dividers with previously reported results.

GaAs HBTs.

5.5.2 Transimpedance amplifier

A circuit diagram of a transimpedance amplifier is shown in Fig. 5-20. Feedback-type amplifiers with a basic common-emitter configuration were designed and fabricated. The circuit consists of a transimpedance gain stage and an impedance matching stage for the output. To ensure good termination of the output, a resistor is inserted in series between the emitter follower and the output pad. Two transistor sizes (Q_1 and Q_3 : $0.5\ \mu\text{m} \times 9.5\ \mu\text{m}$; Q_2 : $0.5\ \mu\text{m} \times 4.5\ \mu\text{m}$) are used. A diode is inserted to bias the HBTs so that they operate around the peak f_T and f_{max} . The transimpedance gain stage has a feedback resistance R_F of $500\ \Omega$ and a load resistance R_L of $1000\ \Omega$. Supply voltages V_{C1} , V_{C2} , and V_E are 11 V, 3.2 V, and -1.5 V, respectively. In order to stabilize the supply voltages, large decoupling capacitors are inserted between the each power supply line and the ground. Figure 5-21 shows a chip micrograph of the fabricated transimpedance amplifier. A $50\text{-}\Omega$ coplanar waveguide transmission line is utilized to connect the resistor used for the termination of the output pad and to achieve good return-loss characteristics. Inputs are directly connected to the input pad in order to avoid inductance and capacitance of the interconnect lines. The chip size is $1.0\ \text{mm} \times 1.4\ \text{mm}$. Most area of the layout is occupied by the decoupling capacitors.

The amplifier was tested on a wafer by using RF probe heads in the frequency range of 45 MHz to 50 GHz. The dependence of transimpedance gain Z_t and output return-loss characteristics S_{22} on the frequency of the transimpedance amplifier is shown in Fig. 5-22. Here, the transimpedance characteristics were calculated from the measured s -parameters. The amplifier has a transimpedance gain of $46.5\ \text{dB} \cdot \Omega$ with a 3-dB bandwidth of 41.6 GHz, and its return loss is below -10 dB over a frequency range of less than 42.0 GHz. The gain-bandwidth product, one of the figures-of-merits for high-speed transimpedance amplifiers, is $8.8\ \text{THz} \cdot \Omega$, and the power consumption is 150 mW.

Figure 5-23 shows the comparison of the gain-bandwidth product versus the power consumption of the fabricated transimpedance amplifier with the previously reported results [29-33]. The power consumption of the developed amplifier is less than half of that of the

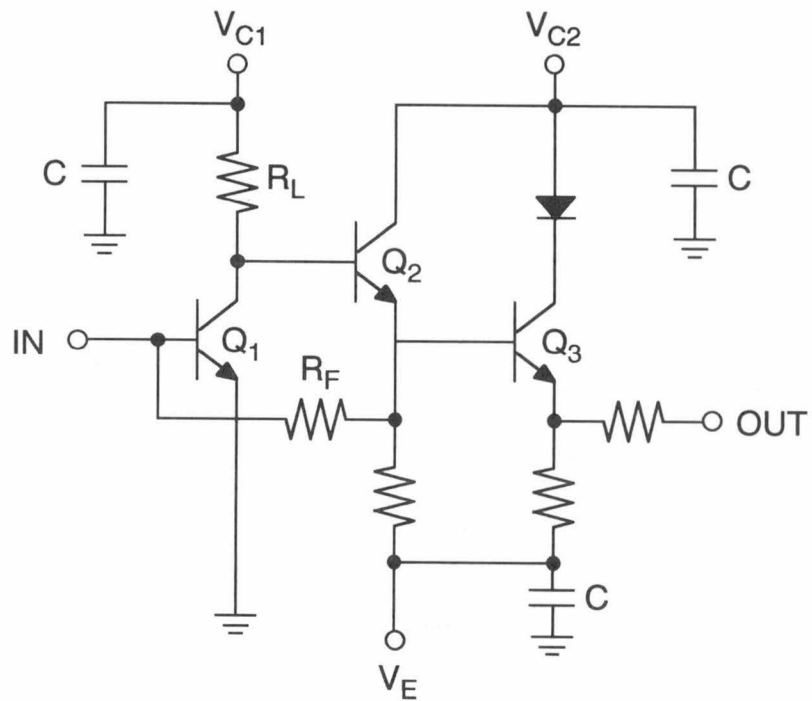


Fig. 5-20. Circuit diagram of the transimpedance amplifier.

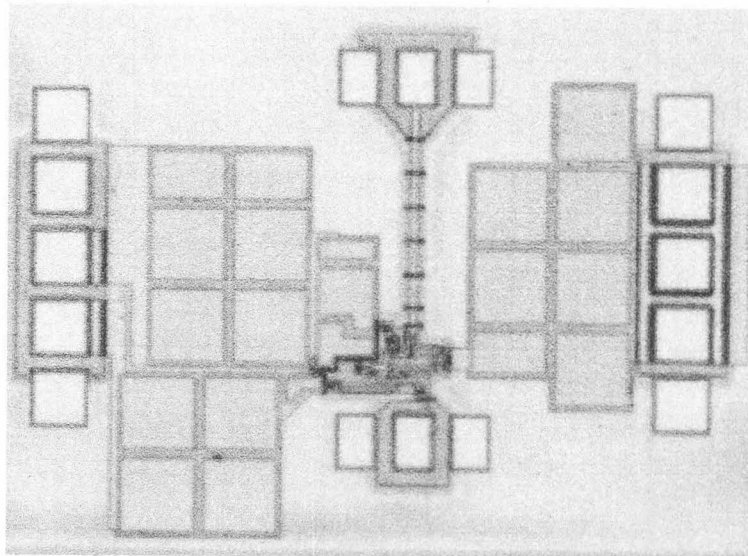


Fig. 5-21. Chip micrograph of the transimpedance amplifier.

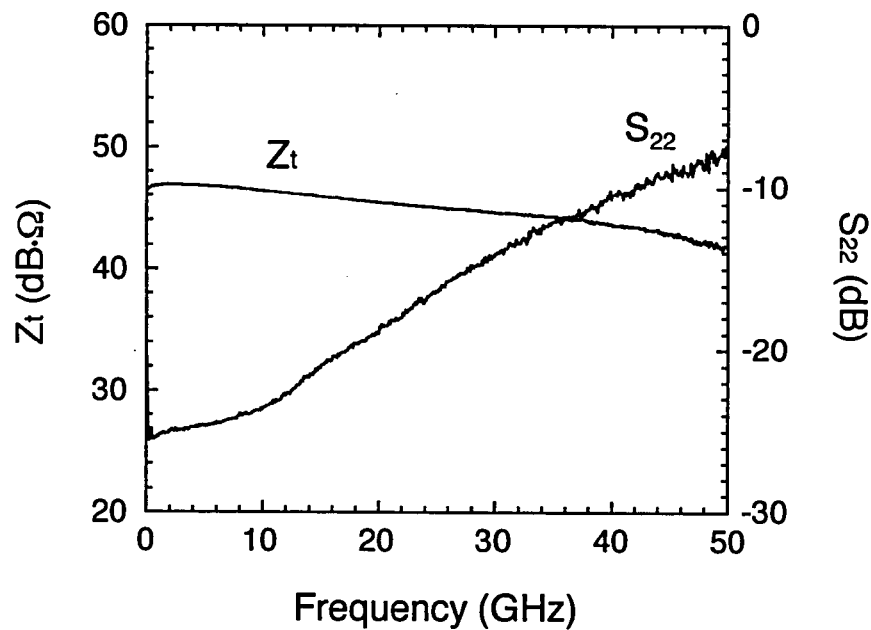


Fig. 5-22. The frequency dependence of transimpedance gain Z_t and output return-loss S_{22} characteristics of the transimpedance amplifier.

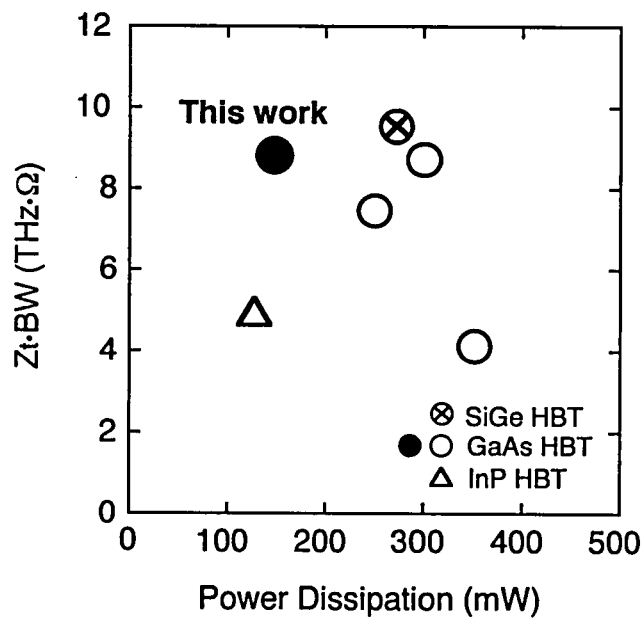


Fig. 5-23. Gain-bandwidth product versus power dissipation of the previously-reported transimpedance amplifiers.

amplifiers fabricated by SiGe and GaAs HBTs at almost the same gain-bandwidth product. On the other hand, the gain-bandwidth product of the fabricated amplifier is almost twice as high as that of the amplifiers fabricated by InP HBTs at almost the same power consumption. These results are due to the higher f_{\max} at lower collector currents of the developed HBTs than those of the previously reported devices, indicating that the developed HBTs are very promising for producing high-speed analog ICs with low-power dissipation.

5.6 Summary

Advanced high-frequency performance of small-scale InGaP/GaAs HBTs with a WSi/Ti base electrode and buried SiO₂ in the extrinsic collector have been demonstrated. The process technology and the device design were refined for further reducing parasitic capacitance at the base-collector junction. A double photoresist coating with a high-temperature reflow improved the uniformity of the buried SiO₂, and improved the thickness of the buried SiO₂ by 25% as well as the device yield to more than 90%. The thick buried SiO₂ together with the reduction of the base electrode area enabled the parasitic capacitance at the buried SiO₂ region to be reduced to 50%.

The improved HBTs by the refinements exhibited much better high-frequency performance with a much smaller emitter size than HBTs demonstrated in chapter 4. An HBT with an S_E of $0.5\ \mu\text{m} \times 4.5\ \mu\text{m}$ exhibited a f_T of 156 GHz and a f_{\max} of 255 GHz at an I_C of 3.5 mA; an HBT with an S_E of $0.25\ \mu\text{m} \times 1.5\ \mu\text{m}$ exhibited a f_T of 114 GHz and a f_{\max} of 230 GHz for at an I_C of 0.9 mA. The developed HBTs had higher frequency operations at lower collector currents with higher breakdown voltage than any other high-performance HBT previously reported.

The developed HBTs were applied to a 1/8 static frequency divider and a transimpedance amplifier. The frequency divider operated at a maximum operation frequency of 39.5 GHz with power consumption per flip-flop of 190 mW, which is about 2/3 of those of previously-reported GaAs-HBT static frequency dividers. The transimpedance amplifier had a transimpedance gain of 46.5 dB·Ω with a 41.6-GHz bandwidth. The power consumption was

150 mW, which is less than half that of the same type of amplifier previously reported.

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Chapter 6

GaAs HBTs with Pseudomorphic GaAsSb Base for Low-Voltage Operation

6.1 Introduction

In chapter 5, the great potential of GaAs-based HBTs for high-speed and low-power operations were demonstrated. However, due to the large bandgap of the GaAs (1.42 eV) [1] used as the base layer, GaAs HBTs have a relatively large turn-on voltage, which limits the minimum operating voltage. For example, the supply voltages of static frequency dividers consisted of SiGe or InP HBTs are 5 – 6 V [2-5], whereas the supply voltages of GaAs HBTs are 6.5 – 8 V [6-8]. The large supply voltage consequently limits the reduction of the power consumption in integrated circuits using GaAs HBTs. In focusing on low-voltage operations, InP or SiGe HBTs are useful because narrow bandgap InGaAs or SiGe is used as the base layer. However, compared to GaAs, InP has the disadvantages of brittleness, unavailability of large-diameter wafers, high substrate cost, and immature process technology with low processing yields, leading to higher production costs. On the other hand, SiGe have the disadvantages of lower breakdown voltage, inferior carrier transport properties, infliction of more loss due to unavailability of semi-insulating substrates. Hence, it is worthwhile to develop GaAs HBTs with a narrow bandgap base layer.

For this reason, GaInNAs has lately attracted considerable attention for use as a narrow bandgap base layer of GaAs HBTs [9-11]. Incorporating small amounts of N into InGaAs significantly reduces the bandgap energy. Moreover, GaInNAs can be grown lattice-matched to GaAs substrates by controlling the In and N compositions. However, since the bandgap difference mainly appears on the conduction band due to the large electronegativity of the N atoms, the large conduction band discontinuity ΔE_C at the emitter-base junction lowers the effect of the narrow bandgap base on the turn-on voltage reduction, as described in chapter 2. Furthermore, the base-collector junction also has large ΔE_C , which blocks electron transport out of the base into the collector. As a result, the current gain is degraded drastically at a high collector current density, which is called the collector current blocking effect [12-14]. Although ΔE_C can be reduced by inserting graded layers between the heterojunctions, this complicates the reproducibility for epitaxial layer growth procedures.

In this thesis, GaAsSb is focused on as a narrow bandgap material for the base layer of GaAs HBTs. The thickness of GaAsSb on GaAs substrates is limited since GaAsSb is not lattice-matched with GaAs. However, GaAsSb offers a definite advantage over GaInNAs: the difference in the bandgap between GaAs and GaAsSb is expected to appear predominantly across the valence band [15]. Hence, the problems occurring in GaAs/GaInNAs systems can be avoided without producing compositionally graded layers. GaAs HBTs with a GaAsSb base have already been demonstrated [16,17]. However, the reduction of the turn-on voltage has not been examined. Furthermore, due to the relatively thick GaAsSb which was well above the critical thickness, the demonstrated devices had many misfit dislocations in GaAsSb, resulting in current gains of less than 10.

In this chapter, GaAs HBTs with a pseudomorphic, fully-strained GaAsSb base are demonstrated. GaAs/GaAsSb/GaAs double heterojunction bipolar transistors (DHBTs) are designed and fabricated so as not to generate misfit dislocations in the GaAsSb layer. The turn-on voltage, the current gain, and the offset voltage of the DHBTs are evaluated and discussed. Characteristics related to the base resistance are also investigated.

6.2 Device Design, Growth and Fabrication

For designing the epitaxial layer structures of GaAs HBTs with a pseudomorphic GaAsSb base, the bandgap energy and the critical layer thickness for misfit dislocation generation of strained GaAsSb lattice-matched to GaAs are estimated first. The bandgap for bulk GaAsSb is given by [18]

$$E_g(\text{GaAs}_{1-x}\text{Sb}_x) = 1.42 - 1.9x + 1.2x^2, \quad (6-1)$$

where x is the Sb composition. Based on this equation, the bandgap energy for pseudomorphic strained GaAsSb is calculated by considering the bandgap shift with hydrostatic stress and the splitting of the valence band given by the deformation potential constants [19]. The critical layer thickness, on the other hand, is calculated by using the formation presented by Matthews and Blakeslee [20]. Figure 6-1 shows the bandgap energy and the critical layer thickness of a strained GaAsSb lattice-matched to GaAs as functions of Sb composition. The bandgap reaches its minimum value of 0.79 eV at an Sb composition x of around 0.8. However, the critical thickness at x of 0.8 is only 2 nm. Although a narrower bandgap is favorable to reduce the turn-on voltage, the extremely thin base is not suitable for the practical use from standpoints of both the fabrication process and the base resistance. Considering both the reduction in the bandgap and the practical base thickness, GaAs_{0.95}Sb_{0.05} and GaAs_{0.9}Sb_{0.1} were utilized as base layers of HBTs in this research. The estimated bandgap energies of GaAs_{0.95}Sb_{0.05} and GaAs_{0.9}Sb_{0.1} are 1.35 eV and 1.28 eV, respectively, and the corresponding critical layer thicknesses are 70.8 nm and 30.7 nm, respectively.

The epitaxial layers were grown on a semi-insulating GaAs (100) substrate by molecular beam epitaxy (MBE) using Si and Be as n - and p -type dopants, respectively. The mole fraction of GaSb was determined from lattice constant measurement by X-ray diffraction and by using the Vegard's law. The actual Sb compositions of the epitaxial layers were confirmed by Auger electron spectroscopy, and the doping concentrations were confirmed by Hall measurements. The parameters of the layer structures are listed in Table

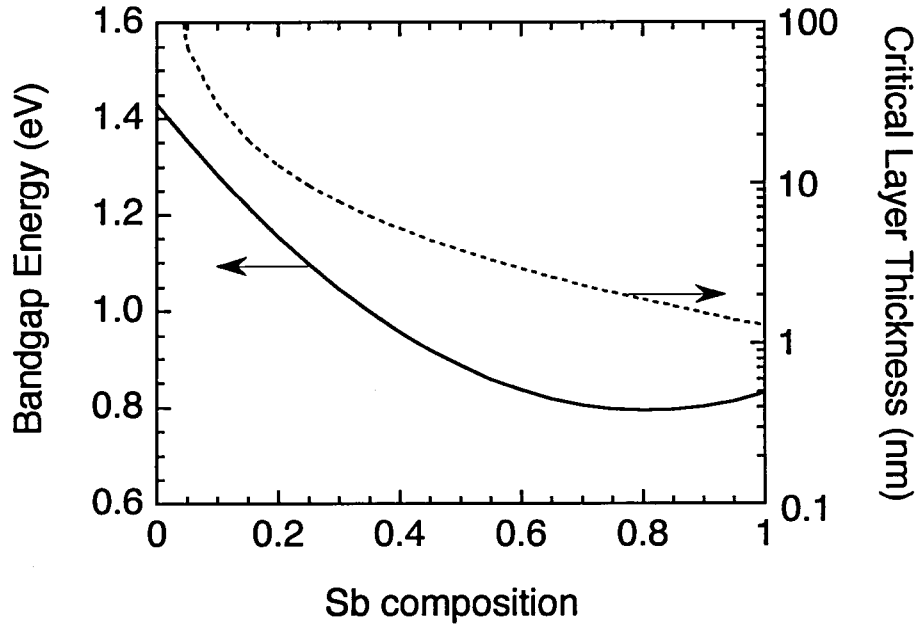


Fig. 6-1. Calculated bandgap energy and critical layer thickness for strained GaAsSb lattice-matched to GaAs as functions of Sb composition.

Table 6-1. Parameters of the epitaxial layer structures of GaAs/GaAsSb HBTs.

Layer	Material	Doping Concentration (cm ⁻³)	Thickness (nm)
Emitter-cap	<i>n</i> -InGaAs	4×10^{19}	50
	<i>n</i> -GaAs	5×10^{18}	100
Emitter	<i>n</i> -GaAs	1×10^{18}	50
Spacer	un-GaAs _{1-x} Sb _x	undoped	2
Base	<i>p</i> -GaAs _{1-x} Sb _x	2×10^{19}	28 ^A , 48 ^{B,C}
Collector	un-GaAs	undoped	150
Subcollector	<i>n</i> -GaAs	5×10^{18}	350
Sb composition	$x = 0.1^{A,B}, 0.05^C$		

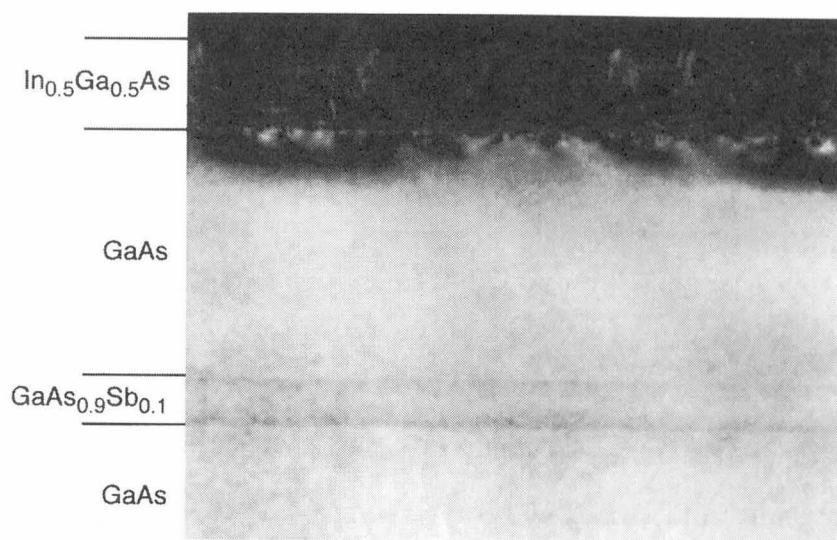
6-1. Three structures were grown for comparison. The Sb composition x of devices A and B was 0.1, and that of device C was 0.05. The p -GaAs_{1-x}Sb_x base layer thickness of device A was 28 nm, and that of devices B and C was 48 nm. A 2-nm undoped GaAs_{1-x}Sb_x spacer layer was inserted between the base and emitter to prevent the p - n junction from shifting towards the emitter layer due to the Be diffusion.

Conventional mesa structure devices were fabricated by using wet chemical etching and a standard photolithographic process. WSi was used as a non-alloyed emitter electrode and an emitter mesa was formed by using the WSi emitter electrode as an etching mask. The base-collector and isolation mesas were formed by using photoresist for the etching masks. The base electrode consisted of Au/Pt/Ti/Mo/Ti/Pt, and the collector electrode consisted of Au/Ni/W/AuGe. They were both formed by lift-off processes and alloyed at 350°C for 30 min. The devices were passivated with SiO₂ by plasma-enhanced chemical vapor deposition at a substrate temperature of 250°C.

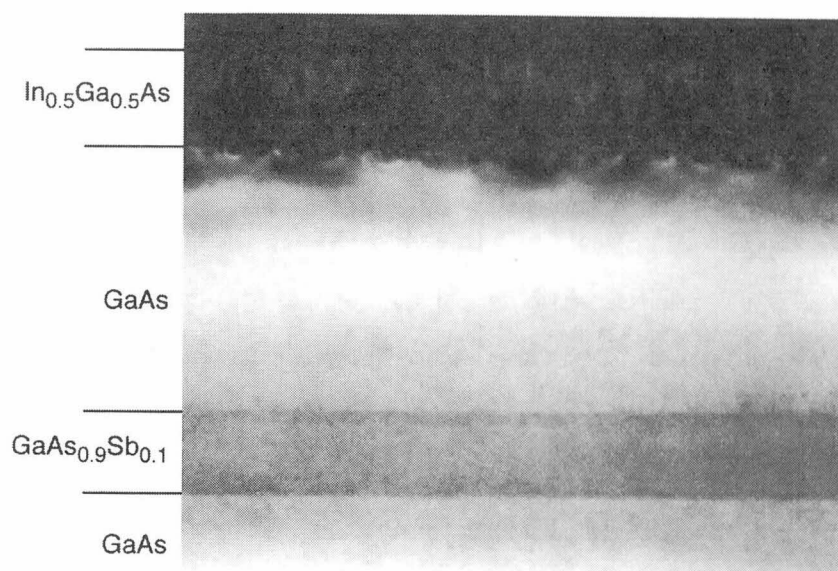
Figure 6-2 shows transmission electron microscopy (TEM) cross sections of the epitaxial layers of devices A and B. No misfit dislocations are observed in both the GaAs_{0.9}Sb_{0.1} layers. In addition, no cross-hatched patterns on the surface morphology were observed by Nomarski interference contrast microscopy. These results indicate that the GaAsSb base layers in the grown HBTs are fully strained. Since the GaAsSb thickness of device B is above the theoretical critical layer thickness, as shown in Fig. 6-1, the real critical layer thickness at the Sb composition of 0.1 is expected being larger than 50 nm.

To evaluate the variation of the bandgap with Sb incorporation, photoluminescence (PL) measurements were performed at room temperature with Ar laser line ($\lambda = 514.5$ nm) excitation. Figure 6-3 shows PL spectra of GaAs/GaAs_{0.95}Sb_{0.05} and GaAs/GaAs_{0.9}Sb_{0.1} HBT epitaxial wafers after removing the InGaAs emitter-cap layers. The peak of the PL wavelength shifts from 0.908 μm (1.366 eV) to 0.944 μm (1.314 eV) with the Sb content increasing from 0.05 to 0.1. The bandgaps evaluated from the peak wavelength are slightly different from those of the calculated values. This is probably ascribed to an error of the estimated Sb composition, which has an error of less than 5%.

Figure 6-4 shows the secondary ion mass spectroscopy (SIMS) profile of the epitaxial layer of device A after device fabrication. Significant Be diffusion towards the emitter layer



(a)



(b)

100 nm

Fig. 6-2. TEM cross sections of the epitaxial layers of GaAs/GaAs_{0.9}Sb_{0.1} HBTs. The GaAs_{0.9}Sb_{0.1} layer thicknesses are (a) 30 nm and (b) 50 nm.

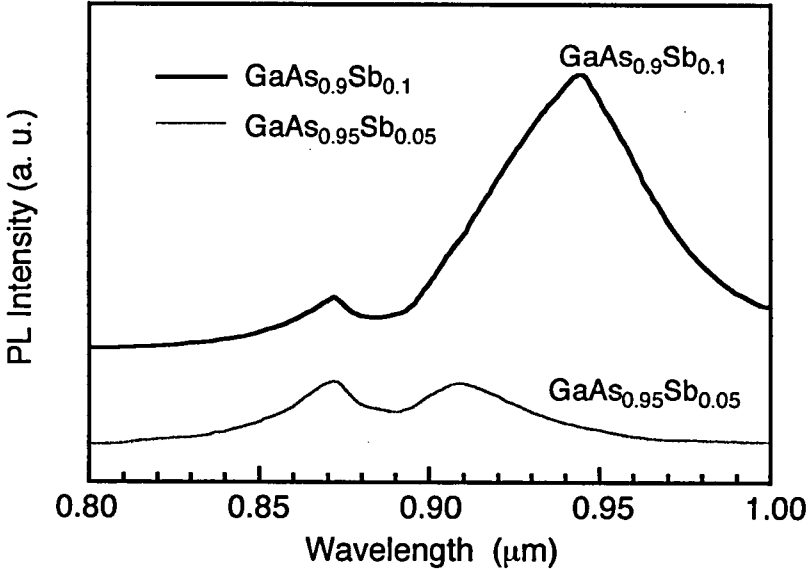


Fig. 6-3. Room-temperature PL spectra of GaAs/GaAs_{0.95}Sb_{0.05} and GaAs/GaAs_{0.9}Sb_{0.1} HBT epitaxial wafers.

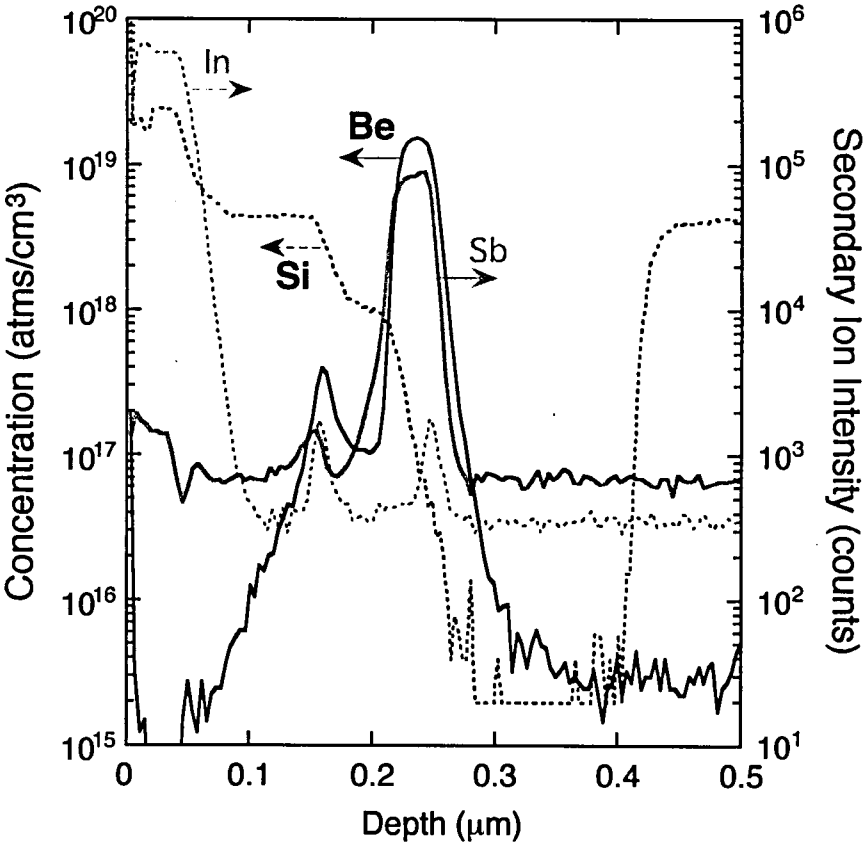


Fig. 6-4. SIMS profile of the epitaxial layer of device A after device fabrication.

over the GaAsSb was not observed. This suggests that the thin GaAsSb spacer layer works effectively and, thus, the influence of Be diffusion during the fabrication process hardly affects on the turn-on voltage.

6.3 Device Characteristics

6.3.1 Turn-on voltage and current gain

The turn-on voltage V_{on} and current gain of the fabricated DHBTs were evaluated from Gummel plots. Figure 6-5 shows the dependence of the collector current density J_C on the base-emitter bias voltage V_{BE} of devices B and C with an emitter size S_E of $100\ \mu\text{m} \times 100\ \mu\text{m}$. Also shown in the figure is the result of InGaP/GaAs HBTs demonstrated in chapter 2 for comparison. The V_{on} decreases as the Sb composition increases. The V_{on} measured at a J_C of $1\ \text{A}/\text{cm}^2$ is $0.984\ \text{V}$ for device B and $1.051\ \text{V}$ for device C. The reduction in V_{on} ($67\ \text{mV}$) by increasing the Sb composition from 0.05 to 0.1 is almost consistent with the reduction in the bandgap estimated by calculation ($70\ \text{mV}$). As explained in chapter 2, this result suggests that ΔE_C at the emitter-base heterojunction is extremely small [21], and, thus, verifies that the bandgap difference mainly appears on the valence band. Furthermore, the V_{on} of device B is about $0.1\ \text{V}$ lower than that of the InGaP/GaAs HBT. These results indicate that GaAsSb is a useful material for reducing the turn-on voltage of GaAs HBTs. As mentioned in the previous section, the theoretical prediction for misfit dislocation generation underestimates the critical layer thickness. Therefore, a much higher Sb composition, and thus, an even lower turn-on voltage, may be achieved without inducing misfit dislocations.

Typical Gummel plots and current gain characteristics for small-emitter devices A and C with an S_E of $3.5\ \mu\text{m} \times 5.5\ \mu\text{m}$ are shown in Fig. 6-6. The maximum current gains of devices A and C are 25 and 6, respectively. The current gain is larger than those of previously reported GaAs/GaAsSb HBTs with the same Sb composition and Gummel number [16]. This is attributed to the pseudomorphic, fully-strained GaAsSb with no misfit dislocations for the fabricated HBTs. Furthermore, the current gains are achieved at a

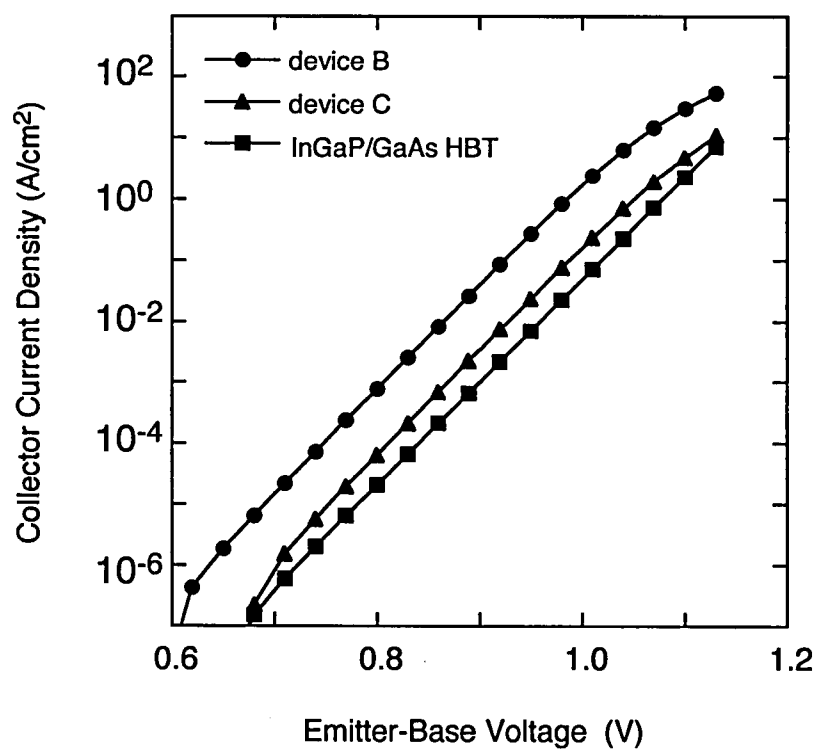
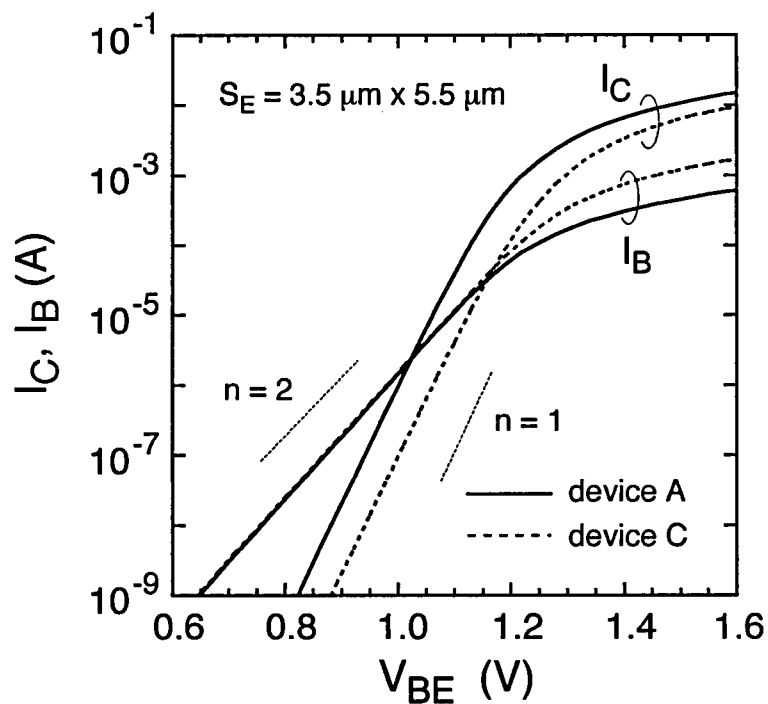
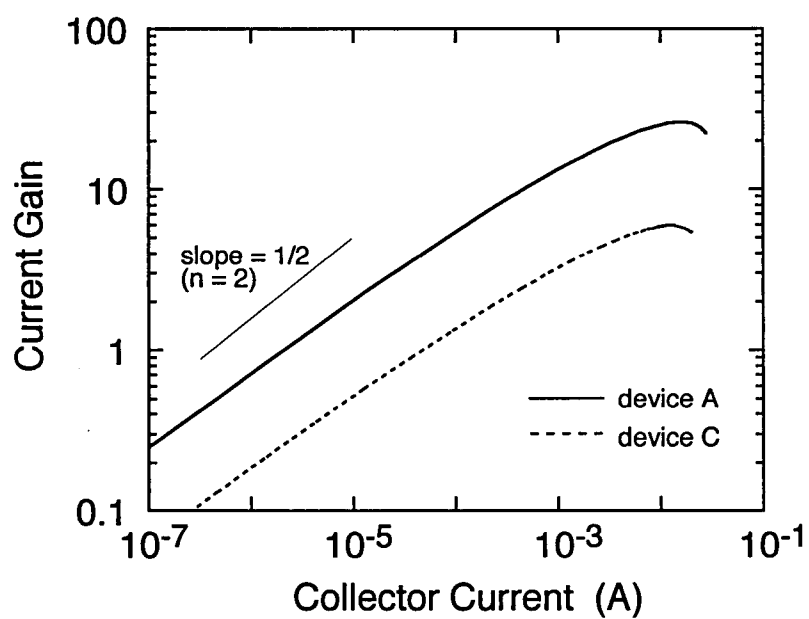


Fig. 6-5. Dependence of collector current density on emitter-base bias voltage of devices B and C with an emitter size S_E of $100 \mu m \times 100 \mu m$. Also shown is the result of InGaP/GaAs HBT demonstrated in chapter 2.



(a)



(b)

Fig. 6-6. (a) Gummel plots and (b) collector current dependence of current gain for devices A and C with an S_E of $3.5 \mu\text{m} \times 5.5 \mu\text{m}$.

relatively high J_C of 8×10^4 A/cm² and do not drop abruptly even at higher J_C . The absence of the abrupt falloff in the current gains verifies that the conduction band discontinuity at the base-collector heterojunction is extremely small. Therefore, the collector current blocking effect, which is a significant problem in DHBTs [12-14], was suppressed in the fabricated DHBTs. The ideality factors of collector and base currents are 1.0 and 2.0, respectively. The large ideality factor of the base currents implies that they are dominated by the recombination at the GaAs emitter depletion regions.

The large base leakage currents were examined in detail by investigating the dependence of the base current on the emitter size S_E . The base current density J_B is written as [22]

$$J_B = J_{Bs} + \frac{L_E}{S_E} J_{Bp}, \quad (6-2)$$

where J_{Bs} is the base current density in the intrinsic base region, L_E is the length of the emitter periphery, and J_{Bp} is the leakage current per unit length at the emitter periphery. Figure 6-7 shows the dependence of J_B on L_E/S_E for the fabricated HBTs at a V_{BE} of 0.8 V, where the ideality factor of I_B is 2. As shown in Fig. 6-7, J_B 's are proportional to L_E/S_E . Furthermore, the J_B 's depend neither on the base thickness nor on the Sb composition. These results indicate that the main component of the base currents with an ideality factor of 2 is J_{Bp} , originating from recombination at the emitter periphery. The large peripheral currents occur probably because the emitter layer consists of GaAs, which has a large surface recombination velocity.

To evaluate the intrinsic current gain of the fabricated HBTs, the size dependence of the base current was investigated at higher J_C . Figure 6-8 shows the dependence of J_B on L_E/S_E at a J_C of 1×10^4 A/cm². The intrinsic current gain $h_{FEi} = J_C/J_{Bs}$ can be evaluated from the y -intercepts in Fig. 6-8, which indicate J_{Bs} . The h_{FEi} values of devices A, B, and C were 35, 23, and 9, respectively. The higher current gain at the larger Sb composition is inferred from the better hole confinement in the base by increasing the valence band discontinuity. In addition, h_{FEi} for the Sb composition of 0.1 is almost inversely proportional to the base thickness. These results suggest that h_{FEi} is limited mainly by the back injection of holes into the emitter, as

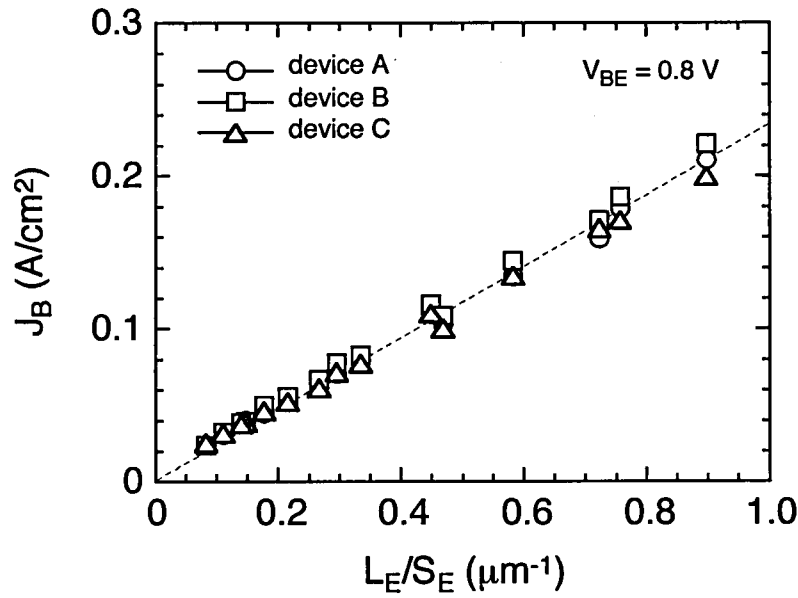


Fig. 6-7. Dependence of J_B on L_E/S_E for the fabricated DHBTs at a V_{BE} of 0.8 V.

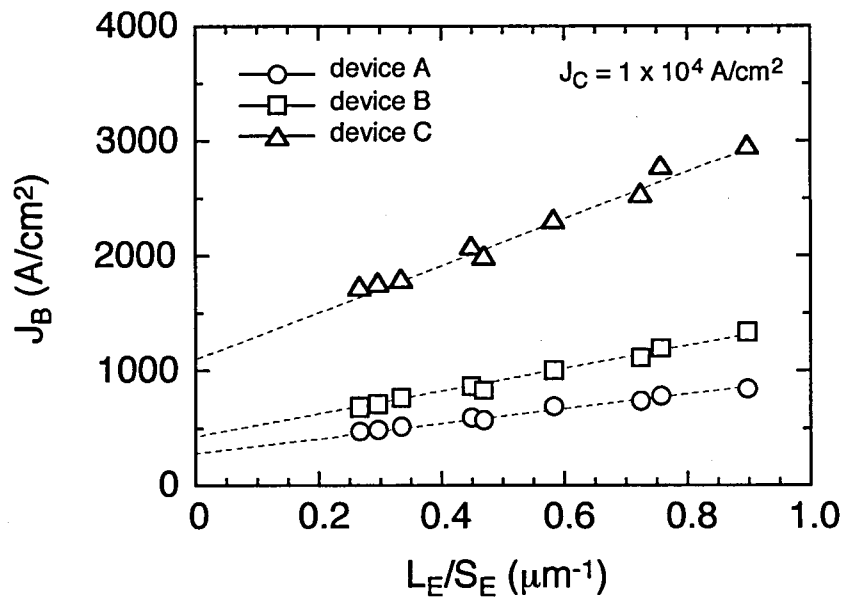


Fig. 6-8. Dependence of J_B on L_E/S_E for the fabricated DHBTs at a J_C of 1×10^4 A/cm².

expressed in Eq. (2-7) in chapter 2. Therefore, the current gains can be improved by increasing the Sb composition.

6.3.2 Knee voltage and offset voltage

The offset voltage V_{offset} is the collector-emitter voltage V_{CE} when the collector current I_C is zero in the common-emitter configuration. The knee voltage V_k is the minimum value of V_{CE} at a given operating I_C . These values are important parameters for HBTs in that small V_{offset} and V_k not only decrease the power consumption in saturating logic circuits, but also increase the active region of operation in analog circuits, leading to high efficiency in power amplifiers.

Figure 6-9 shows the common-emitter $I_C - V_{CE}$ characteristics of device A with an S_E of $3.5 \mu\text{m} \times 5.5 \mu\text{m}$. At an I_C of larger than 10 mA, current gain decreases with increasing V_{CE} because of an effect that is associated with an increase in junction temperature owing to the increased power dissipation [23]. Despite using the abrupt base-collector (BC) heterojunction, a small V_k of 0.48 V is attained at a relatively high J_C of $5 \times 10^4 \text{ A/cm}^2$. The small V_k under high-current-density operation is attributed to the extremely small potential spike at the BC heterojunction that blocks electron transfer [24-26]. In contrast, V_{offset} is about 0.10 V, which is relatively large despite the symmetry of the epitaxial layers in DHBTs [24].

To investigate the cause of the large V_{offset} , V_{offset} for the fabricated DHBTs of device A with various transistor sizes was examined. The V_{offset} is generally expressed as [27,28]

$$V_{offset} = R_{EE} I_B + \frac{kT}{q} \ln\left(\frac{S_C}{S_E}\right) + \frac{kT}{q} \ln\left(\frac{J_{Cs}}{\alpha_{CE} J_{Es}}\right), \quad (6-3)$$

where R_{EE} is the emitter resistance, S_C the size of the BC junction, α_{CE} the forward current gain, and J_{Es} and J_{Cs} the emitter and collector saturation currents, respectively. In this equation, the component of the BC forward current with an ideality factor $n = 2$ is not considered [29,30]. This is because, as shown in Fig. 6-10, the BC forward current I_{BCF} is dominated by the bulk diffusion current with $n = 1$ at current densities J_{BCF} above $1 \times 10^2 \text{ A/cm}^2$ (base-collector bias voltage V_{BC} above 1.1 V), on which bias conditions V_{offset} is

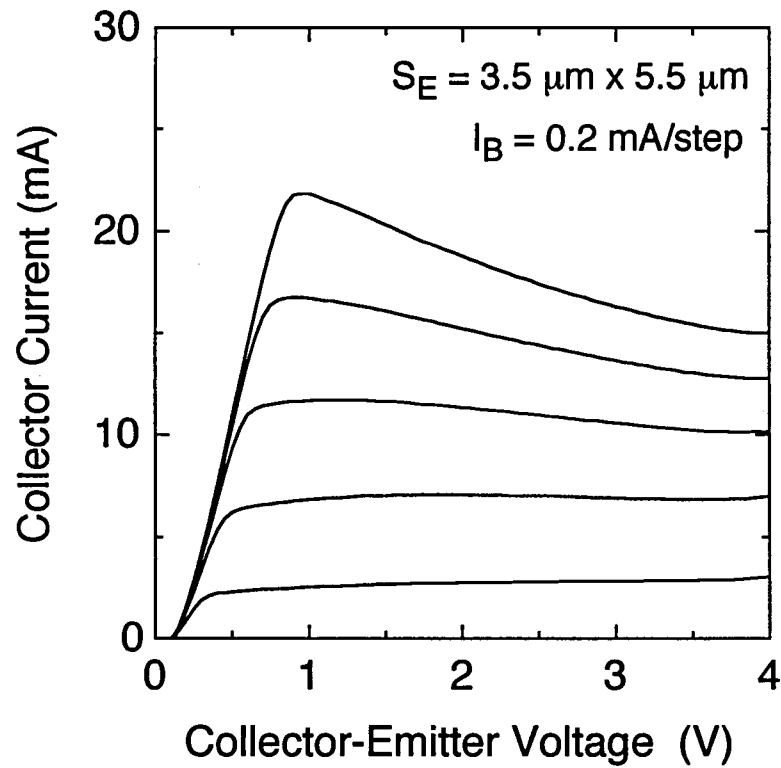


Fig. 6-9. Common-emitter $I_C - V_{CE}$ characteristics of device A with an S_E of $3.5 \mu\text{m} \times 5.5 \mu\text{m}$. The curves are taken in base-current steps of 0.2 mA .

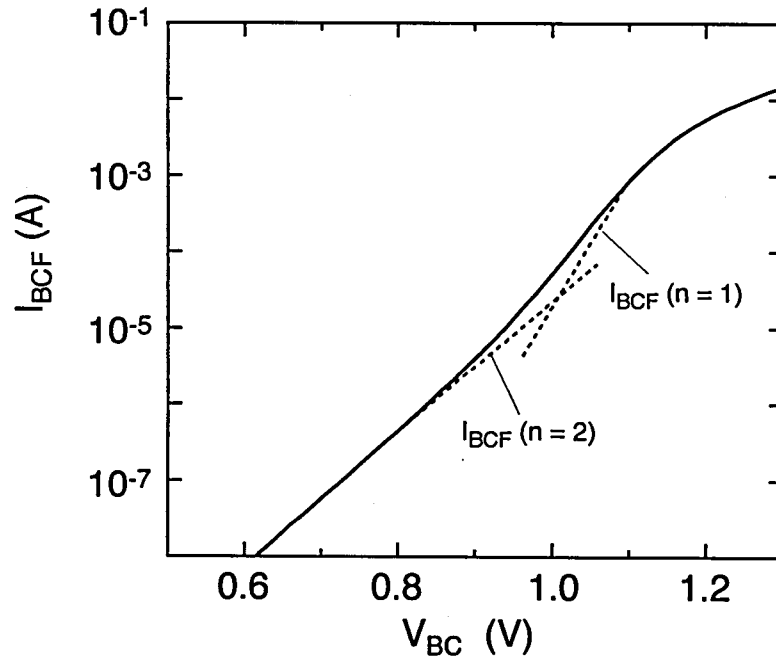


Fig. 6-10. Dependence of BC forward current I_{BCF} on BC bias voltage V_{BC} for device A with a BC junction size S_C of $25 \mu\text{m} \times 40 \mu\text{m}$. The $I_{BCF}(n=1)$ is obtained by subtracting the extrapolated $I_{BCF}(n=2)$ from the measured I_{BCF} .

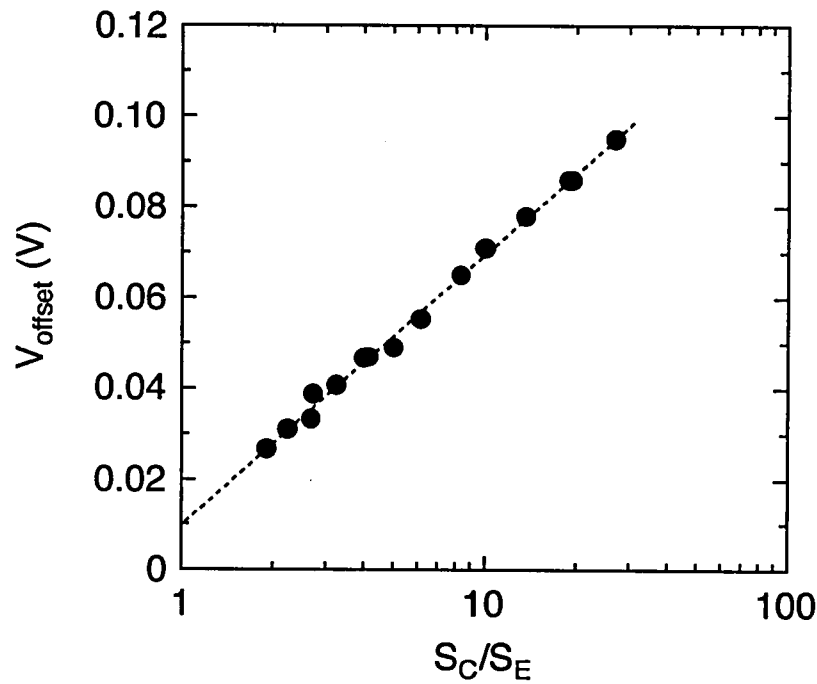


Fig. 6-11. Offset voltage V_{offset} , measured at a J_B of $1 \times 10^3 \text{ A/cm}^2$, as a function of collector-to-emitter area ratio S_C/S_E .

evaluated. Figure 6-11 shows the V_{offset} , measured at a base current density J_B of 1×10^3 A/cm², as a function of collector-to-emitter area ratio S_C/S_E . The value of the product $R_{EE} \times I_B$ was evaluated to be 0.5 mV. Therefore, the y-intercept (10 mV) in Fig. 6-11 originates mainly from the difference in turn-on voltage between the emitter-base junction and the base-collector junction, given by the third term of the right side of Eq. (6-3). As the S_C/S_E increases, the second term of Eq. (6-3) becomes the dominant factor in V_{offset} , as shown in Fig. 6-11, and thus becomes the cause of the large V_{offset} in Fig. 6-9. Since the non-self-aligned process was used, the S_C/S_E ratio of the fabricated DHBTs drastically increased when the emitter size was scaled down. For example, S_C/S_E is 2.7 and V_{offset} is 0.04 V when $S_E = 20 \mu\text{m} \times 50 \mu\text{m}$, while S_C/S_E is 27 and V_{offset} is 0.10 V when $S_E = 3.5 \mu\text{m} \times 5.5 \mu\text{m}$. Therefore, the V_{offset} of small-scale devices can be further decreased by fabricating devices using a self-alignment process, which brings S_C/S_E close to unity.

6.3.3 Contact Resistance and Sheet Resistance of Base

Finally, characteristics associated with the base resistance were investigated. The specific contact resistance ρ_c and the sheet resistance ρ_s of the base layers were evaluated by using the standard transmission line model (TLM) method [31,32].

Figure 6-12 shows ρ_c for $p\text{-GaAs}_{1-x}\text{Sb}_x$ and $p\text{-GaAs}$ as a function of carrier concentration N_B . The results of theoretical calculations based on a tunneling model are also plotted by dashed lines [33]. The calculations were carried out for various potential barrier heights ϕ_B assuming an effective light hole mass of $0.082 m$ [1,34], where m is the mass of the free electron. The value of ϕ_B has a tendency to decrease as the Sb content increases. This is probably attributed to the shift of the pinning position of the surface Fermi level toward the valence-band edge resulting from the inclusion of Sb [35,36]. As a result, a ρ_c as low as $6 \times 10^{-7} \Omega \cdot \text{cm}^2$ was achieved at $x = 0.1$ (devices A and B) with a relatively low N_B of $2 \times 10^{19} \text{ cm}^{-3}$. This low ρ_c enables to reduce the area of the base contact, and thus the base-collector capacitance without sacrificing an increase in the contact resistance, which effectively improves high-frequency characteristics, as discussed in chapter 4.

The ρ_s values of devices A, B, and C, in contrast, were 2.30, 1.35, and 1.13 k Ω /square,

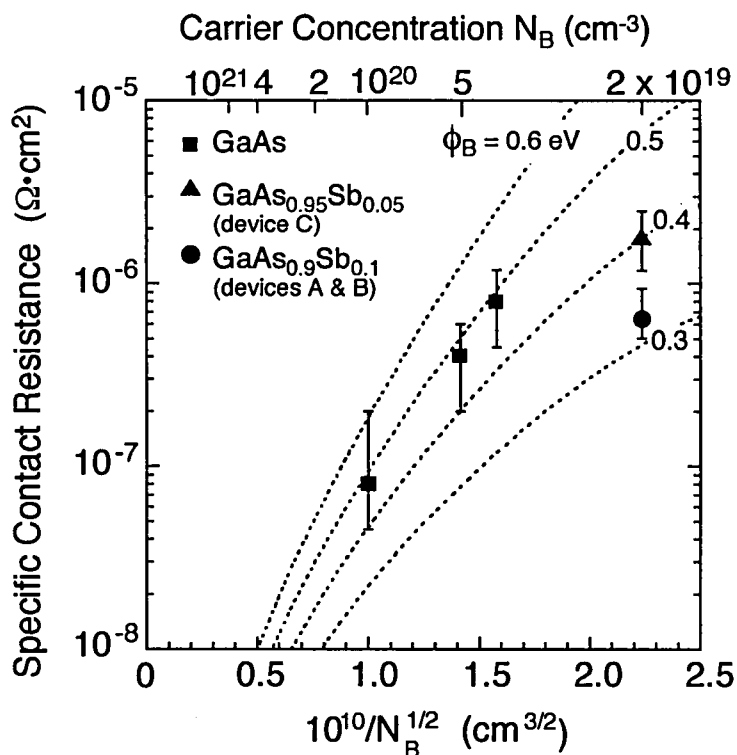


Fig. 6-12. Specific contact resistance ρ_C of $p\text{-GaAs}_{1-x}\text{Sb}_x$ and $p\text{-GaAs}$ as a function of carrier concentration N_B . The results of theoretical calculations based on a tunneling model are also plotted by the dashed lines.

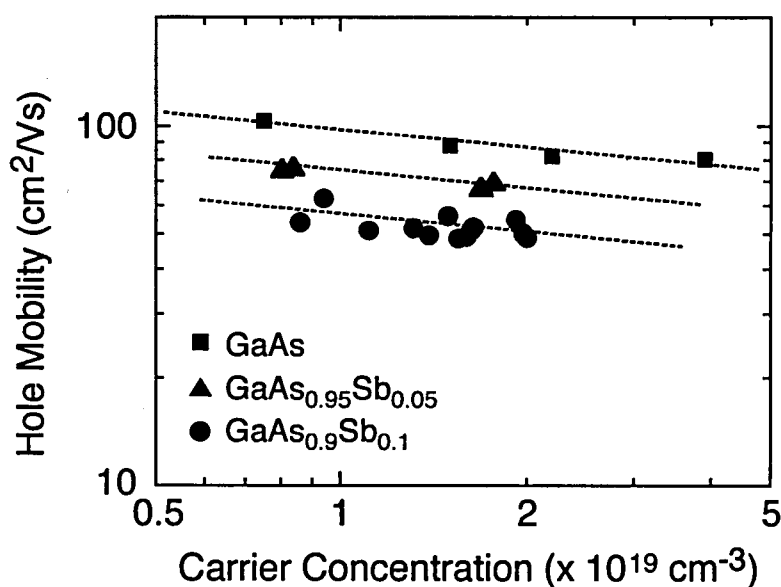


Fig. 6-13. Hole mobility of $p\text{-GaAs}_{1-x}\text{Sb}_x$ and $p\text{-GaAs}$ as a function of carrier concentration.

respectively, which are larger than those for p -GaAs estimated from same doping levels and thicknesses. Figure 6-13 shows the dependence of hole mobility on the carrier concentration for p -GaAs_{1-x}Sb_x and p -GaAs by Hall measurements. The mobility decreases as the Sb composition increases. The low mobility, and thus the large sheet resistance, is probably ascribed to the alloy scattering in ternary materials [37]. To reduce the sheet resistance for the high-speed operations, therefore, p -GaAsSb with much higher doping concentration should be developed.

6.4 Summary

For reducing the turn-on voltage V_{on} in GaAs HBTs, a pseudomorphic, fully-strained GaAsSb was applied to the base layer. The V_{on} of the GaAs/GaAs_{0.9}Sb_{0.1} HBTs was reduced by about 0.1 V compared to that of the InGaP/GaAs HBT. The reduction was in good agreement with the bandgap reduction of the base layer, suggesting that the bandgap difference mainly appears on the valence band. Owing to the fully-strained GaAsSb without misfit dislocations, the maximum current gain of 35 was attained, which is higher than those of previously-reported GaAs/GaAsSb HBTs. TEM cross-sections showed that no misfit dislocations were observed in GaAs_{0.9}Sb_{0.1} layers even though the thickness was above the theoretical critical layer thickness, indicating that a much higher Sb composition and, thus, much lower turn-on voltage may be achieved without inducing misfit dislocations.

The maximum current gains reached at a relatively high collector current density J_C of 8×10^4 A/cm² without abrupt drop at higher J_C . In addition, the small knee voltage V_k of 0.48 V was obtained at a relatively high J_C of 5×10^4 A/cm². These results suggest that the collector current blocking effect of the fabricated DHBTs is insignificant due to the extremely small conduction band discontinuity ΔE_C .

The potential barrier height of metal/ p -GaAsSb tended to decrease as increasing the Sb content. As a result, a specific contact resistance as low as 6×10^{-7} $\Omega \cdot \text{cm}^2$ was achieved at p -GaAs_{0.9}Sb_{0.1} with a relatively low base doping level of 2×10^{19} cm⁻³. In contrast, the hole mobility of GaAsSb was increased as the Sb composition increased, which may be ascribed to

the alloy scattering in ternary materials.

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Chapter 7

Conclusions

7.1 Conclusions

This thesis has referred to novel technologies of GaAs HBTs for high-speed and low-power applications. A series of the novel technologies dealt with analyses of material properties, fabrication processes, device designs, and circuit applications, those were developed to overcome the crucial problems of GaAs HBTs for high-speed and low-power operations. The main conclusions of this thesis are summarized as follows.

In chapter 2, the characteristics of conventional InGaP/GaAs HBTs were evaluated and analyzed in detail in order to exploit InGaP/GaAs HBTs for use in high-speed and low-power applications. The abrupt InGaP/GaAs HBTs had almost the same turn-on voltage as a graded AlGaAs/GaAs HBTs. In addition, the emitter size effect of InGaP/GaAs HBTs was smaller than AlGaAs/GaAs HBTs. These results indicate that InGaP/GaAs is a useful material system for fabricating small-scale GaAs HBTs with low turn-on voltage. The delay time analysis showed that the main component of the delay was the intrinsic transit time τ_F , which effectively decreased by reducing the base thickness. In contrast, the dominant factors for smaller devices were parasitic delays, τ_E and τ_{CC} , which increased because the extrinsic collector region to contact the base electrode and the wire was not reduced when the emitter size was scaled down.

In chapter 3, the characteristics of InGaP/GaAs HBTs with a heavily-doped and thin base are studied in detail in order to optimize the base layer design for high-speed operations. The dependence of the current gain h_{FE} on the base doping concentration N_B showed that the h_{FE} at an N_B of less than $3 \times 10^{20} \text{ cm}^{-3}$ was determined by Auger recombination in the intrinsic base region, which was inversely proportional to the square of N_B . In contrast, the h_{FE} at an N_B above $3 \times 10^{20} \text{ cm}^{-3}$ decreased drastically because of the increase in the back injection of holes. The dependence of h_{FE} on temperature revealed that the effective hole barrier height ΔE_{Veff} decreased as N_B increased. The reduction of ΔE_{Veff} was explained analytically and experimentally by considering the bandgap narrowing and the Fermi level in accordance with the Fermi-Dirac distribution. The dependences of h_{FE} and the intrinsic transit time τ_F on the base thickness W_B showed that the τ_B exhibited a quadratic dependence on W_B at a W_B larger than 30 nm, whereas the τ_B tended to show a linear dependence at a smaller W_B . Accordingly, reducing W_B is effective for reducing the τ_B , and thus τ_F , at W_B of larger than 30 nm; whereas W_B of less than 30 nm is not effective, at which τ_B occupied less than 1/3 in τ_F .

In chapter 4, a novel device structure and the corresponding process technology were proposed to remove the GaAs in the extrinsic collector underneath the base contact pad region. The devices were fabricated by using WSi/Ti as the base electrode and by burying SiO₂ in the extrinsic collector region under the base electrode. The specific contact resistance ρ_c of WSi for *p*-GaAs was $2 \times 10^{-6} \Omega \cdot \text{cm}^2$ at an N_B of $1 \times 10^{20} \text{ cm}^{-3}$. The ρ_c was dramatically reduced to $3 \times 10^{-7} \Omega \cdot \text{cm}^2$ by inserting a 5-nm Ti film between the interface. The low ρ_c made it possible to reduce the optimum base contact width for achieving both high f_T and high f_{max} to less than 0.4 μm without the large increase in the base resistance. The fabricated device structure exhibited that the WSi/Ti base electrode is useful to cover both the narrow base contact surface and the buried SiO₂ outside of the base-collector junction. Small-scale devices demonstrated excellent high-frequency characteristics at low collector currents: an HBT with an S_E of $0.6 \mu\text{m} \times 4.6 \mu\text{m}$ provided an f_T of 138 GHz and an f_{max} of 275 GHz at an I_C of 4 mA; and an HBT with an S_E of $0.3 \mu\text{m} \times 1.6 \mu\text{m}$ provided an f_T of 96 GHz and an f_{max} of 197 GHz at an I_C of 1 mA. The developed HBTs had higher-speed and lower-current operation than the conventional HBTs, verifying that the simultaneous reduction of both the emitter size and the extrinsic collector capacitance was effective to improve the high-frequency performance of

small-scale GaAs HBTs.

In chapter 5, the advanced high-frequency performance of small-scale InGaP/GaAs HBTs with the proposed device structure was demonstrated. The base-collector capacitance was further reduced by refining the process technology and the device design. A double photoresist coating with a high-temperature reflow improved the uniformity of the buried SiO₂, and improved the thickness of the buried SiO₂ by 25%. The thick buried SiO₂ together with the reduction of the base electrode area enabled the 50% reduction of the parasitic capacitance at the buried SiO₂ region. The refinements improved the high-frequency performance of HBTs with much smaller emitter sizes. An HBT with an S_E of $0.5\ \mu\text{m} \times 4.5\ \mu\text{m}$ exhibited a f_T of 156 GHz and a f_{max} of 255 GHz at an I_C of 3.5 mA; an HBT with an S_E of $0.25\ \mu\text{m} \times 1.5\ \mu\text{m}$ exhibited a f_T of 114 GHz and a f_{max} of 230 GHz for at an I_C of 0.9 mA. The capability of the developed HBTs for high-speed and low-power integrated circuits was also investigated by applying them to 1/8 static frequency dividers as digital circuits and transimpedance amplifiers as analog circuits. The static frequency divider operated at a maximum operation frequency of 39.5 GHz with power consumption per flip-flop of 190 mW, which is about 2/3 of those of previously-reported GaAs-HBT static frequency dividers. The transimpedance amplifier had a transimpedance gain of $46.5\ \text{dB} \cdot \Omega$ with a 41.6-GHz bandwidth. The power consumption was 150 mW, which is less than half that of the same type of amplifier previously reported.

In chapter 6, GaAs HBTs with a pseudomorphic, fully-strained GaAsSb base were demonstrated. GaAsSb was applied as the narrow bandgap base material for reducing the turn-on voltage V_{on} in GaAs HBTs. The V_{on} of the GaAs/GaAs_{0.9}Sb_{0.1} HBTs was reduced by about 0.1 V compared to that of the InGaP/GaAs HBT. The reduction was in good agreement with the bandgap reduction of the base layer, indicating that the bandgap difference mainly appears on the valence band. Owing to the fully-strained GaAsSb without misfit dislocations, the maximum current gain of 35 was attained. TEM cross-sections showed that no misfit dislocations were observed in GaAs_{0.9}Sb_{0.1} layers even though the thickness was above the theoretical critical layer thickness of 50 nm. The collector current blocking effect of GaAs/GaAsSb/GaAs DHBTs was insignificant due to the small conduction band discontinuity ΔE_C and, consequently, the small knee voltage V_k of 0.48 V was obtained at a relatively high J_C

of 5×10^4 A/cm². The potential barrier height of metal/*p*-GaAsSb tended to decrease as increasing the Sb composition. As a result, a specific contact resistance as low as 6×10^{-7} Ω·cm² was achieved at *p*-GaAs_{0.9}Sb_{0.1} with a relatively low base doping level of 2×10^{19} cm⁻³. In contrast, the hole mobility of GaAsSb was increased as the Sb composition increased, which may be attributed to the alloy scattering in ternary materials.

7.2 For the Future Work

As stated in the previous section, the novel technologies studied in this thesis demonstrated great potential of GaAs HBTs for high-speed and low-power integrated-circuit applications. However, there still remains room for the improvements of characteristics.

As for the subject on reducing turn-on voltage V_{on} , the reduction of V_{on} demonstrated in chapter 7 is insufficient compared to the lower V_{on} of SiGe or InP HBTs. Hence, the increase in the Sb composition of GaAsSb is indispensable. In this case, the GaAsSb layer must be thinned in order to avoid suffering from misfit dislocations. In addition, to suppress the increase in the base resistance due to the thin base, the doping concentration must be simultaneously increased, which can be materialized by using carbon as the *p*-type dopant [1,2]. The deep understanding for a heavily-doped and thin base layer acquired in this research will be useful for designing the epitaxial layer of the GaAsSb base.

GaInNAs is another possible choice of the base material for reducing V_{on} . GaInNAs can be grown lattice-matched to GaAs substrates by controlling the In and N compositions and, consequently, reduces the turn-on voltage of GaAs HBTs to less than 1.0 V [3-6]. However, the bandgap can be changed substantially even though the compositions are slightly varied. Therefore, accurate controllability of the epitaxial growth is a significant issue for the practical use of GaInNAs to the base layer of HBTs.

As for the subject on high-speed IC operations, the relaxed layout design for wiring of GaAs process is a remaining problem. Despite lower f_T and f_{max} of SiGe HBTs than GaAs HBTs, SiGe HBT digital circuits have demonstrated higher frequency performance because of the high integration due to the advanced wiring process. Therefore, the wiring process should be

improved to fully exploit the high-frequency characteristics of GaAs HBTs.

For the further improvement of the high-frequency performance of small-scale GaAs HBTs, reduction in parasitic resistance is indispensable. Although the emitter resistance are not seen any size effect, as shown in Fig. 5-1(a) in chapter 5, the large resistance itself affects the increase in the parasitic delay. Optimization of the emitter-cap and emitter layer designs will effectively improve the performance [7]. In addition, since the developed HBTs have the highest $f_T - BV_{CEO}$ product, the collector layer design should also be optimized.

Information technology is now continuously progressing with the tremendous increase of communication capacity. Therefore, the requirement of high-speed devices with low-power operation will be further raised in the future. The author believes that the developed technologies will also play a wide role in the developments of further high-speed and low-power devices by applying them to other heterostructure devices as well as InP HBTs, and contribute to the highly developed communication society in future.

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List of Publications

A. Full length papers and letters

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